Breakthrough Packaging Technology Achieves Fully Enabled High Speed & High Density Packaging of Power GaN & SiC

A Technical Synopsis of IP Purchase Opportunity

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The proprietary Semiconductor Packaging Solutions μMaxPak technology offers quantum improvements for high speed, high voltage and high power devices in near chip-scale surface mount (SMD) packages. These performance improvements are enabled by extremely low inductance, electrical resistance, and thermal resistance. The proprietary architecture is leadless and wire-bondless, and accommodates vertical integration of cascode switches, gate drivers, magnetic isolators and other functions/components. The μMaxPak is ideal for high power 600V & 1200V switches, and these advantages become essential for wide band-gap (WBG) power devices at larger currents and higher speeds. The μMaxPak architecture is protected by U. S. patent 9,214,416 issued 12/15/15, and key to evolving GaN & SiC power device operation at optimum performance & efficiency, and even improves performance & efficiency of high speed Si power devices. The μMaxPak implementation can be Laminate-based LGA or Leadframe-based QFN/DFN with lateral or vertical power die, and is compatible with existing commercial assembly technology and equipment. The numerous technology benefits are broad & scalable, enabling higher efficiency & power density for diverse applications. The near chip-scale μMaxPak architecture virtually eliminates WBG package performance constraints, and is enables direct die-to-Cu interface of smaller WBG power die. Furthermore, SMD devices that are under-filled, coated or potted are absolutely the best way to manage high voltage (HV) spacing/creepage and system integration, which are required for increased power-densities.

μMaxPak Enables Half-Bridge with 5x5mm Die

Ultra-Fast GaN & SiC Switching	>100 MHz
Negligible + to - Inductance	<0.1 to 0.2nH
Ultra Low + to - Resistance	<100 to 200μohm
Low Thermal Resistance, Die-Case	0.1^{o}C/W
Switching Voltage Scalable to	>2,000Vp
High Temperature Operation, Tj(max)	>185^{o}C
Maximum Efficiency for GaN & SiC to	>99%

Accommodates HV IEC, EN & UL Pollution 1 External Pad Spacing with under-fill, coating or potting

Displaces many Hi-Power Hi-Voltage DBC Modules

Multi-chip Die Switches are Ideal, SS, HB FB, etc.

Vertical/3D Topology with integrated cascode, gate-drivers & other components

Optimum Wide-Band die yield with pre-tested building blocks for Power PCBs or DBC Modules

Reduced Package NRE, Risk & Development Time

Low Cost QFN Leadfame or Laminate Platform

HV Power GaN Applications:

Present: 200-650V @ 10-50A for PFC, Solar Inverters & Power Supplies (TO220/247 & Limited leadless SMD)

Near-Term: EV/HEV, UPS & Industrial Motor Drives are increase to 100s of Amps

Future Potential: Add 1200V & increase current further

HV Power SiC Applications:

Present: 1200V & Up @ 50-100A Solar Inverters, P.S. & UPS. (TO220/247 & diodes in DBC modules)

Near-Term: Industrial Motor Drives & Traction with Full (FET/Diode) SiC DBC modules at increasing speed, and at current to hundreds of amps & thousands of volts

Future Potential: EV/HEV, Wind Turbine & Electric Grid with ever increasing currents & voltage

HV Power Si Applications:

Advanced and Evolving Fast IGBTs & Power HV FETs in all existing applications

Package Innovation & µMaxPak Patent

The µMaxPak packages are near-chip-scale SMD molded packages, and typically Dual- or Quad-Flat-No Lead (DFN or QFN) packages with open power die cavity(s) in bottom of package. The bottom cavity(s) offer direct mechanical, thermal & electrical connection between exposed power die and user mother-board or substrate, and the leadframe or laminate copper makes thermal and electrical connections between the top-side of power die and additional package bottom pads. The cavity allows double-side leadframe or laminate assembly with top-side available for vertical integration with bump-chip or SMD components like cascode switches, gate drivers, isolators and other components, or in some configurations direct top-side heatsink or cold-plate. The Figures 1, 2 & 3 architectures show leadframe-based µMaxPaks, but are equally applicable to laminate-based µMaxPaks.

Figure 1: µMaxPak Single-Switch (SS) Cross-section showing vertical power FET die in bottom-side leadframe cavity with gate & source connected to leadframe, and gate drive IC output connected to top of FET gate pad.

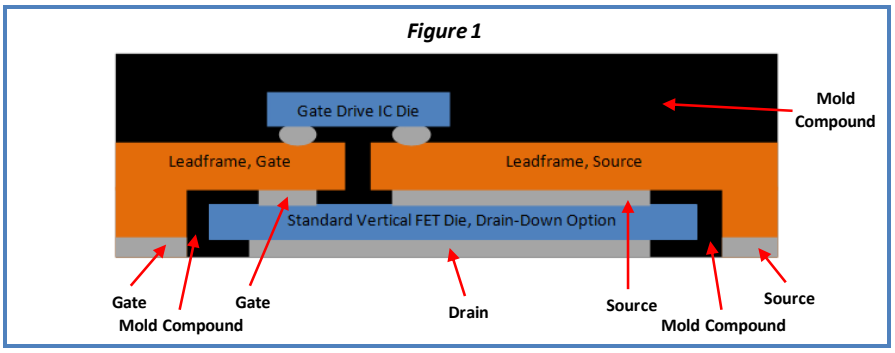


Figure 2: µMaxPak Single-Switch Cross-section showing inverted vertical power FET die in bottom-side leadframe cavity with drain connected to leadframe.

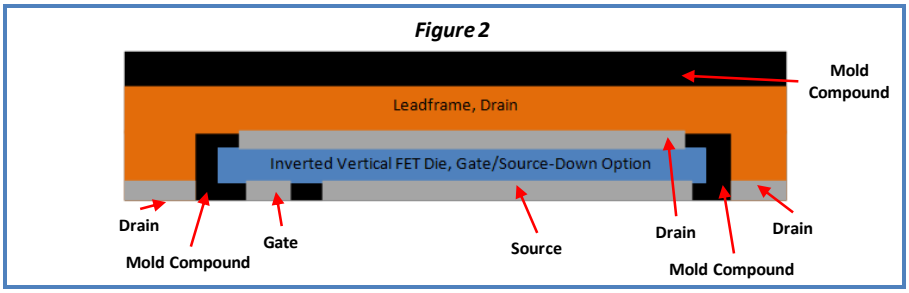
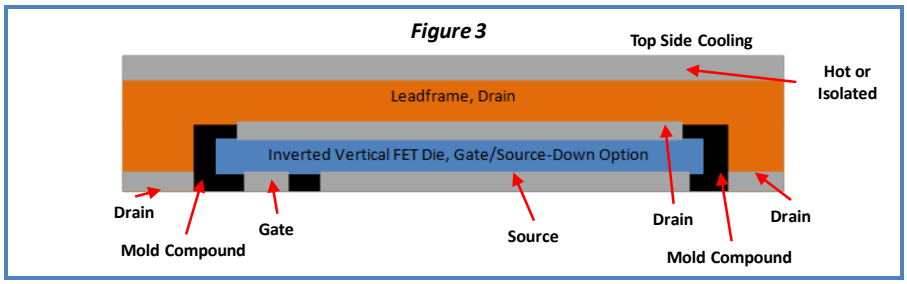


Figure 3: Rugged leadframe structure showing inverted vertical power FET die in bottom-side leadframe cavity with drain connected to leadframe, which can be clamped between top & bottom cold plates for high power dissipation in applications like EV/HEV.



Power die can be a) lateral or vertical, b) normally-on or normally-off, and c) Si, SiC or GaN, and all connections can be bump-pad (No WBs). This structure provides geometrically ideal high-current interconnects with virtually zero length, and maximum copper width and thickness. This accommodates gate driver outputs sitting directly above switch gate & sense pads. The tight near chip-scale die packaging is ideal for paralleled die, and offers significantly better performance if HB, FB & 3-Phase switches are co-packaged.

Laminate-based μMaxPak best accommodates complex interconnects at low to medium power, and Leadframe-based μMaxPaks are most rugged providing lowest R, L and Rjc for higher power & higher switching speeds.

The well controlled and proven DFN/QFN processes/materials can accommodate HV external pad separation for UL pollution 1 minimum spacing for voltage to 1200Vp and higher, allowing high package power-densities to be extended to the mother-boards, modules or full systems.

The μMaxPak IP is protected by U.S. Patent, "High Speed, Low Loss and High Density Power Semiconductor Packages (μMaxPak) with Molded Surface Mount High Speed Devices(s) and Multichip Architectures(s)". The patent shows numerous examples of μMaxPak configurations including:

- Standard & Inverted Die
- Vertical & Lateral Die
- Diode, IGBT, FET, JFET & BJT Die
- Leadframe & Laminate (LGA) based packages
- Single-Switch & Half-Bridge (Half-Bridge is preferred/optimum)
- Vertical Integration of Cascode FET, Gate-Driver IC & passive components
- Thin Type architecture with leadframe exposed on both top & bottom for extreme ruggedness and maximum power dissipation.
- The unique and proprietary μMaxPak architecture can be assembled on commercial standard assembly lines, thereby reducing cost, risk and development/startup time.

The μMaxPak architecture's near zero packages Rjc must be used on thermal mother-boards to fully utilize their potential. Laminate power PCBs with heavy Cu, thermal via, thermal pre-preg, embedded heat-slugs are practical and economical, and at the highest power levels DBC mother-boards are required. The Power PCB and DBC can be enhanced with heatsinks and convection at higher power levels, and in some cases the

μMaxPak can be used as pre-tested building blocks for conventional high power DBC modules.

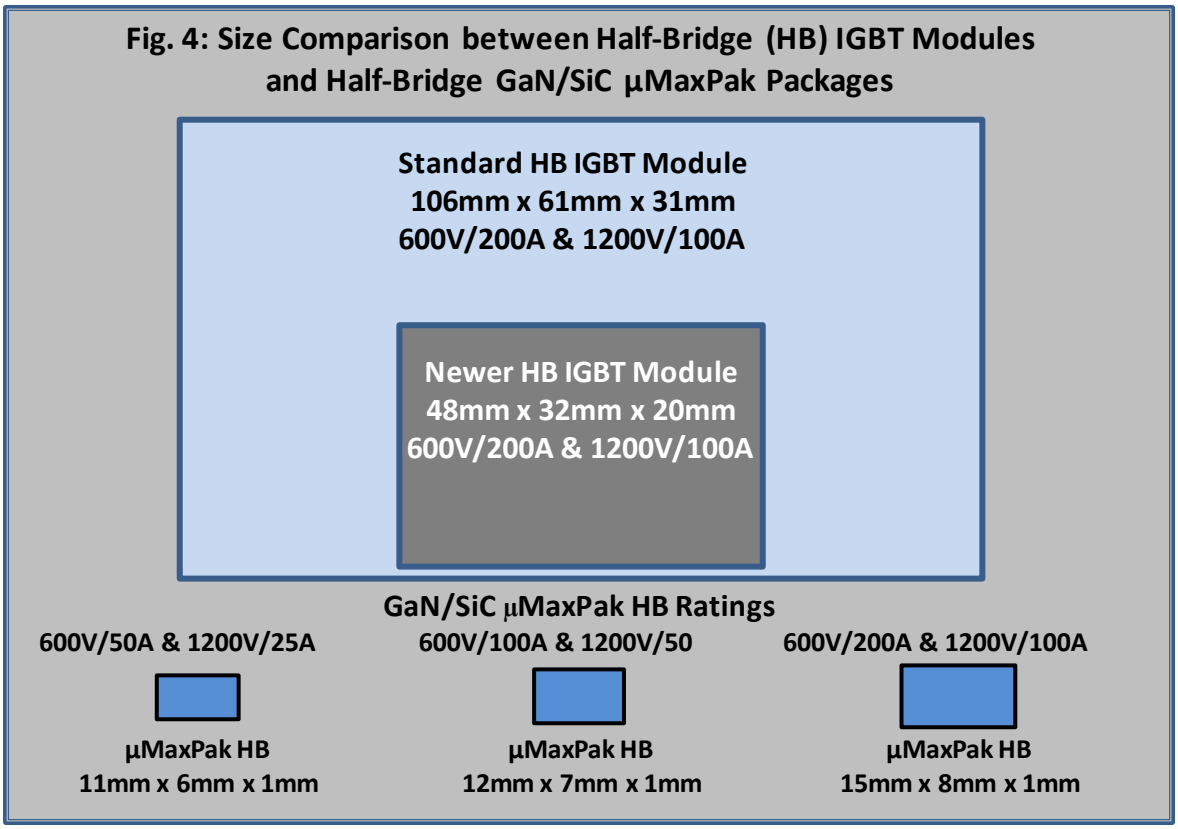
Competitive Advantages

WBG Package Type Package Architecture	D²Pak&TO220-247 Custom Multi-Chip	LGA QFN Lamiante-Based	Power PQFN LF w Solder Clip	μMaxPak Laminate-Base	μMaxPak Leadframe-Base
Parasitcs(L)	High	Moderate	Low	Very Low	Near-Zero
Package Losses(R)	High	Moderate	Low	Low	Lowest
Thermals(Rjc)	Low	Moderate	Low	Low	Lowest
Power Density	Low	Moderate	High	High	Highest
SMD	D2Pak only	YES	YES	YES	YES
Leadless	NO	YES	YES	YES	YES
Wire Bondless	NO	YES & NO	YES	YES	YES
Max BV	600/1200(TO247)	600/1200	600/1200	600/1200	600/1200
Max.Current, 600V(2)	<50A(D2Pak/TO220)	<50A	50A	150A	200A
Max.Current, 1200V(1)	50A(TO247)	<50A	<50A	75A	100A
Switches, Potential	SS	SS/HB/FB/3P	SS/HB	SS/HB/FB/3P	SS/HB/FB/3P
Integration, Potential	Cascode	Cascode/GD/isol/etc	Cascode	Cascode/GD/isol/etc	Cascode/GD/isol/etc
Complexity	High	Moderate	Moderate	Low	Lowest
Manufacturability	Fair	Good	Poor	Good	Good
Value	Poor	Fair	Poor	Good	Best
Cost	Marginal	Low	High	Low	Low

NOTES:
1. **μMaxPak is a proprietary DFN/QFN architecture offered with package constraints shown.**
2. **Typical maximum continuous GaN & SiC currents of available HV SiC & GaN products.**
3. **μMaxPak highlighted parameters are as good as or better than the best competing packages.**
4. **To accommodate GaN and SiC, the TO-220, D2Pak, TO247, and PQFN assemblies are non-std & complex with multi-components, isolators, etc.**

Power Density

The μMaxPak power-density is enabled by improvements in die power-density & efficiency. If we assume GaN & SiC die power-density are increased by a factor of 10 and losses reduced by a factor of 5, the potential μMaxPak sizes with 5x5mm power die are shown in Figure 4 with standard 600/1200V IGBT modules. These assumptions are conservative, relative to the potential of wide band-gap power devices. Today most Power GaN & SiC devices are being sold for lower currents & operating frequencies, and usually in leaded TO220 & TO247 packages, despite the introduction of a number of leadless laminate & leadframe based SMDs. Still, the μMaxPak enables the best available improvements in both Power-Density & Performance.



(Approximate Actual Size Shown)

Courtney Furnival of Semiconductor Packaging Solutions has over 30 years in high volume semiconductor packaging experience. He also has 10 years experience designing custom DFN & QFN packages for high-power, high-voltage and high frequency applications that include power MOSFET, Power ICs, and IGBT modules for major companies, and has designed numerous power GaN & SiC packages for key companies in recent years. The proprietary μMaxPak architecture is a direct extension of this experience. He has successfully managed a number of high volume production facilities during those years. With that experience, he has very effective guided Asian packaging houses from prototype designs through pilot runs to full production for various top industry semiconductor companies. This guidance included maximizing throughput, quality, and reliability, while minimizing cost. Courtney Furnival holds a bachelor degree in Physics, with minors in Chemistry, and Mathematics. He has completed his course work towards a PhD in Physics. He started his work in a Power and RF electronic packaging material and process R &D center. Courtney Furnival holds numerous patents on power modules and semiconductor packages, and special processes and manufacturing techniques of electronic high volume packages.

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