Inevitability of Near Chip-Scale SMD Packaging for Power GaN & SiC

Frequently-Asked-Questions About Ultimate WBG Near Chip-Scale SMD Packaging

Today's performance of power Wide Band-Gap (WBG) devices is severely limited by conventional power packages (i.e. TO220, TO247 & IGBT DBC-modules). We are seeing some early Power QFN and LGA WBG packages with modest improvements, but they are still performance limiting and are costly. Future higher performance power WBG evolution will simply not be possible without Near Chip-Scale SMD packages. Such Near Chip-Scale SMD packages are absolutely required for power WBG device's potential power density, performance, speed, efficiency and costs.

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There is a symbiotic relationship between power WBG devices and Near Chip-Scale SMD packages, or more specifically these packages enable power WBG and power WBG enable Near Chip-Scale packages. Inevitability of Near Chip-Scale power WBG packaging can be better understood by looking at the example of today's digital microprocessor's integration and packaging. In principle, hundreds of thousands of transistors could be packaged as discretes, and soldered together, but such a maze of leads and interconnects would have unacceptable parasitics, size, reliability and cost. Discrete microprocessors would just not be possible. Going one step further, the proprietary µMaxPak package architecture is an optimum example of Ideal Near Chip-Scale packaging. The following Frequently-Asked-Questions provide insight into the benefits of WBG Near Chip-Scale package capability and its Ultimate form, the µMaxPak package technology.

Q1: Are Near Chip-Scale SMD Packages Really Inevitable for Power WBG devices?

A1: Yes they are Inevitable. Near-Chip-Scale SMD packages are small, leadless & wire bondless, approaching the size of the chips enclosed. They are essential for Full performance of power WBG devices, because they reduce parasitics and thermal resistance (Rjc). Thereby improving WBG speed, efficiency, reliability & costs, and they allow similar improvements to the overall system. The µMaxPak is an example of Ultimate Near Chip-Scale WBG packaging.

Q2: What are the Primary Performance Advantages of the µMaxPak packages?

A2: The µMaxPak is the ultimate implementation of the Near Chip-Scale packaging concept, because it minimizes parasitics and maximizes heat transfer. This is accomplished by minimizing current loop path length with leadless and wire bondless packages. Thus enabling power WBG devices to operate at maximum efficiency by reducing both conduction & switching losses. Furthermore, the exceptionally low package thermal resistance Rjc enhances reliability and increases maximum current rating. Table 1 quantifies potential performance advantages for µMaxPak half-bridges with WBG die size between 5mm x 5mm and 7mm x 8mm.

Package Parameters	Values
Negligible Loop-Inductance	L < 0.1-0.2 nH
Negligible Loop-Resistance	R < 100-200 µohm
Ultra-Fast GaN & SiC Switch	f > 100 MHz
Virtually Zero Common Source-Inductance	0
Thermal Resistance, Die-to-Case	Rdc < 0.1 C^0/W
High Temperature Operation	Tj(max) = 185^{0}C

Table 1: Primary QFN-µMaxPak Performance Advantages.

Q3: If more Efficient WBG devices reduce Power Dissipation, why is lower Package Thermal Resistance required?

A3: Although higher WBG efficiencies are reducing power dissipation significantly, the WBG die power densities are increasing about twice as fast as efficiencies. Therefore, thermal resistance per unit area must be reduced. The basic µMaxPak packages utilizes robust Cu conductors and reduced solder interfaces to more effectively remove heat from both top & bottom of the die. For very high power dissipation products, more heat can be removed with heatsinks or cold-plates on both the top & bottom of the package. Looking to the future, potentially GaN & SiC operating temperatures will increase, further enhancing heat dissipation.

Q4: Why have Chip-Scale SMD packages not been used for Power Si IGBT modules?

A4: Si IGBT modules require very large IGBT & diode die. Such large die cannot be soldered directly to Cu leadframes, because of large coefficient of thermal expansion (CTE) mismatch between Cu and die. This is acceptable for smaller die where we see smaller discrete IGBT & diode die soldered directly to Cu leadframes or to the bases of TO220 & TO247 packages, but the much larger IGBT die in modules require a DBC CTE buffer between die and base plate.

Q5: Why can Higher Current SiC and GaN die be used Directly on Cu?

A5: Power SiC and GaN die can have 10 times the current density of Si IGBT die, which enables die to be 1/10th the size. Therefore, WBG devices in Near Chip-Scale SMD packages can be soldered to Cu leadframes and operate at hundreds of amperes.

Q6: What are the basic Types or Structures of µMaxPak Architecture?

A6: The µMaxPaks are molded, leadless and wirebondless SMD packages, like the QFN and LGA packages. They uniquely can accommodate double-sided assembly of the internal leadframe or substrate. The double-sided assembly is made possible by the Proprietary Bottom-Side Cavity(s) Architecture.

Standard Type 1 QFN-µMaxPak packages have the power die soldered into the bottom cavity(s) of the QFN leadframe (or LGA substrate) with the die gate (G) & source (S) pads soldered to the leadframe, leaving the die drain (D) pad(s) exposed at the bottom of the package. The Type 1 configuration is Ideal for Vertical Integration with additional components on the top of the leadframe (or substrate). These components can include bump-chip gate-drivers (GD), isolators and passive components. The cross-section in Figure 1 is a Type 1 example with a vertical WBG die in the bottom cavity and GD IC on top of the leadframe.

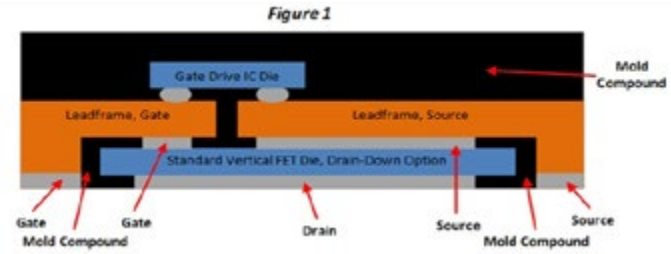

Figure 1: Type 1 example with a vertical WBG die in the bottom cavity and GD IC on top of the leadframe.

Inverted Type 2 QFN-µMaxPak packages have the power die soldered into the cavity(s) in the bottom of the leadframe (or substrate), but with the D pad(s) soldered to the leadframe and the G & S pads exposed at the bottom of the package. The Inverted Type 2 µMaxPak allows horizontally integrated gate-drivers, which can be external or internal (Horizontal gate-driver options not shown). See cross-section in Figure 2.

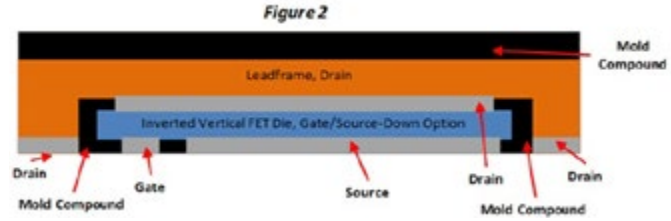

Figure 2: Inverted Type 2 µMaxPak allows horizontally integrated gate-drivers.

Thin Type 3 QFN-µMaxPak packages are Inverter Type 2 µMaxPak with the leadframe also exposed at the top of the package. They are robust, and accommodate both top & bottom heatsinks. They are well suited for EV Inverters, which are usually clamped between top & bottom cold plates. See cross-section in Figure 3.

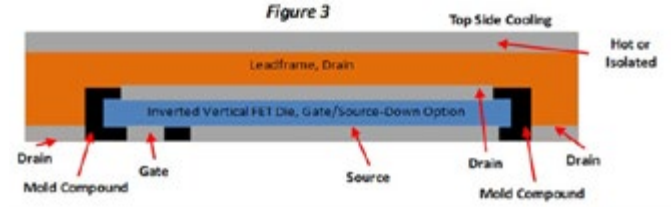

Figure 3: QFN-µMaxPak packages are Inverter Type 2 mMaxPak

Q7: Why use modified QFN µMaxPak packages for power WBG packaging?

A7: The QFN structure is simple, robust, reliable and low cost. The mature commercial QFN/DFN package technology is flexible, and available at many contract assemblers. Its flexibility allows easy size and layout customization without hard tooling, allowing packages to be optimized for each product configuration, optimizing performance and reducing tooling NRE, design/process risk, and new product time-to-market. These advantages are built on inherent features like being leadless and wire bondless, with a heavy single piece Cu leadframe that provides connections from the top of the die to the bottom-side pads. These features contribute to the exceptionally low inductance, electrical resistance and thermal resistance.

Q8: Why are Chip-Scale µMaxPak QFN packages so Cost Effective?

A8: The QFN packages are small, and they have simple internal structures with one-piece leadframe. They do not require internal DBC for CTE buffer, and they do not require complex external leads and terminals. Existing Power QFN packages often replace wire bonds with solder clips, increasing assembly complexity, NRE, interfaces, cost, size and reliability risks. The proprietary µMaxPak architecture eliminates solder clips and easily accommodates multi-chip configurations like half-bridge (HB), full-bridge (FB) and 3-phase bridge (3P).

Q9: What are the differences between Leadframe-Based and Substrate-Based µMaxPak?

A9: Leadframe and Substrate µMaxPak use the same proprietary architecture having die cavities(s) on the bottom of the package and components or supplementary heatsink/cold-plate on the top. Although QFN are LGA packages, and LGA can be QFN packages, it is common to call Leadframe µMaxPak packages “QFN” and Substrate µMaxPak packages “LGA.”

Q10: What are pros & Cons of QFN versus LGA µMaxPaks?

A10: Leadframe-Based QFN µMaxPaks utilize thicker and wider Cu interconnects, creating an optimum 3-D geometry. This provides the lowest current-loop-inductance, lowest current-loop electrical resistance, and is mechanically more robust. It also provides the lowest thermal resistance (Rjc), and highest heat capacity to better accommodate repetitive peak power pulses. The simple one-piece leadframe assembly provides lower costs than the LGA-µMaxPak. Substrate-Based LGA µMaxPaks also have low current loop-inductance and low electrical resistance, but not as low as the QFN µMaxPak. Their substrates are PCBs or laminates, and use high temperature laminate materials with Cu foil and Cu via for electrical and thermal connections. Since Cu foil and via are not as heavy as solid Cu leadframes, electrical and thermal internal connection of the LGA µMaxPaks can never perform quite as well as QFN µMaxPaks. That said, since both µMaxPak packages have exposed die pads on the bottom of the package as primary heat dissipation path, the thermal resistance Rjc of the LGA µMaxPak is still nearly as good. LGA substrates can provide thinner traces and more complex interconnects, which allows more complex circuitry and vertical integration. Circuit density can be further increased in LGA µMaxPak by embedding passive component in the laminate substrate.

µMaxPak Packages	Loop-Inductance	Loop-Resisatnce	Rjc (Thermal Resistance)	Simple & Robust	Vertical Integration	Integration Complexity	Assembly Costs
QFN	Lowest	Lowest	Lowest	Very Good	Yes	Basic	Lowest
LGA	Low	Low	Low	Good	Yes	High	Medium

Table 2: Comparison, QFN-µMaxPak versus LGA-mMaxPak.

Q11: Can µMaxPak Architecture accommodate both Lateral and Vertical WBG die?
A11: Yes it can. The Vertical die structure is most common for power SiC, and ideal for Near Chip-Scale packaging, because all power pads provide both electrical and thermal external connections, and they provide the best high-voltage separations with D pads on one side and S/G pads on the other.
Power GaN die are typically Lateral structures with all electrical connections on the top-side of the die, while the other side contain only thermal pads. With G, S & D on the same side, the pads are smaller and the high voltage spacing (S to D) must be large, which can limit maximum current and voltage.
An exception is GaN-on-SiC die, which can accommodate thru-SiC via to bring the D to the other side. GaN-on-SiC is more expensive today, but better thermally.

Q12: Can µMaxPak accommodate both Normally-Off and Normally-On WBG die?
A12: Yes it can, but Normally-On die does increase package complexity. Normally-On die are typically managed with a Cascoded circuit, which requires a low-voltage MOSFET die in series with the high-voltage WBG die, and extra internal connection(s). Normally-Off die are easiest to manage. Today most power WBG die are Normally-Off. However, Cascoded switches can have advantages in some applications?

Q13: How are Signal Pads and Connections managed in µMaxPak?
A13: WBG power and signal die pads vary by manufacturer, ratings and product. Therefore, it is recommended that the die pads and µMaxPak pads be co-designed for performance, manufacturability and reliability. Ideally all connections will be soldered to the QFN leadframe pads or LGA foil pads. Signal pads often include gate, sense and current sense pads. External signal pads will be different with integrated gate driver(s).

Q14: Can µMaxPak packages accommodate Multiple WBG power die?
A14: Yes it can. The µMaxPak architecture can accommodate single or multiple WBG switches, and each switch can accommodate paralleled WBG die and anti-parallel diodes. Common configurations for multiple switch µMaxPak can be HB, FB and 3P, and they can be easily customized for special configurations. FB and 3P are best suited for lower power levels, and at higher power levels it can be more practical to create them with multiple HB packages. In general, the Half-bridge provides higher power density and lower current-loop inductance than two single-switches. An example of a SiC µMaxPak HB is shown in Figure 4A (Cross-Section) and Figure 4B (Bottom-side pads). This HB structure has a non-inverted high-side power die and an inverted low-side power die enabling it to be directly soldered on the positive bus & negative bus to minimize loop-inductance.

Figure 4a: HB Cross-Section View

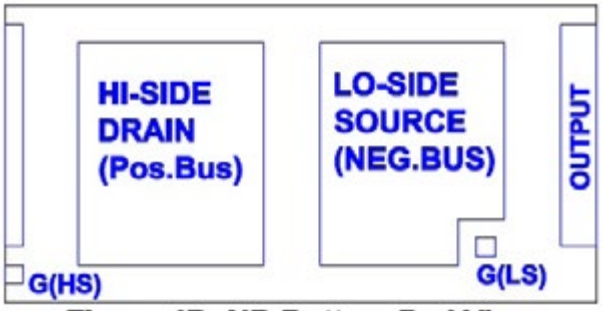

Figure 4b: HB Bottom Pad View

Q15: Are µMaxPak packages suitable for Higher WBG Operating Temperatures?
A15: GaN can operate at higher temperatures than Si, and SiC at higher temperatures than GaN. Today's power GaN and SiC devices are usually not operated above 150°C, being primarily limited by increased Rds(on) at higher junction temperatures, but both WBG materials can accommodate much higher operating temperatures as WBG devices evolve.
The µMaxPak package operating temperature can be limited by the choice of solder and molding compound, and by CTE mismatch. LGA µMaxPak packages can additionally be limited by choice of substrate laminate material.
Today's typical QFN & LGA materials can accommodate temperatures Tj(max) of 185°C, with typical Sn/Ag/Cu solders, Hi-Tg molding compounds, and laminates like BT resins. There are higher temperature materials available today, which can allow µMaxPak Tj(max) up to about 225°C in the µMaxPak packages

Q16: Is it true that µMaxPak technology Improves System Architecture and Performance?
A16: Yes it does. The small & thin packages significantly reduce system size and weight. Smaller power SMD packages can be placed close together eliminating heavy leads, bulky terminals and large spacing/creepage distances. This reduces Integrated System size, weight and cost. The total current loop-inductance and resistance of integrated system interconnects are typically larger than that of the packages. The µMaxPak packages virtually eliminate most high current/voltage internal connectors and interfaces. Furthermore, tighter control, feedback and protection circuitry are more easily implemented.

Q17: Are UL/EN isolation & Safety Regulations met by Near Chip-Scale packages?
A17: Yes, the smaller UL minimum spacing & creepage distances are already used inside traditional power Si IGBT modules, where die, traces and passive chips are small & thin, allowing easier coating or potting. Likewise the small and thin µMaxPak packages make coating, potting and under-fill much easier, especially in enclosed integrated systems. Under-fill, coating and potting materials must be suitable for Pollution Degree 1 minimum spaces & creepage distances, like those used inside traditional high power Si IGBT modules.

In Summary:
Power WBG (GaN & SiC) devices need Near-Chip-Scale SMD packages to reach today's WBG devices full performance, efficiency and power density potential. Inevitably such packages will be absolutely required as power WBG devices evolve toward the inherent potential of GaN & SiC materials. Increased WBG power density and efficiency has enabled new packages like the µMaxPak, and the µMaxPak packages enable the power WGB full performance, efficiency and power density. Furthermore, Near Chip-Scale µMaxPak packages reduce unit cost, tooling NRE and new product time-to-market. These packages are compatible with standard QFN & LGA assembly technologies, which are reliable, robust and available today. Small SMD packages can also simplify System structures increasing system performance, efficiency and power density, and reducing system cost.

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