

**Edward Herbert Designs**

# **Switched Current Power Converter**

## **Transient and Frequency Response**

Revised March 5, 2006

*Solutions for*

*Advanced Performance*

*Power Supplies*

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**On behalf of Edward Herbert  
For more information, contact:**

**Arnold Alderman  
Anagenesis, Inc.      Tel: 310 662 4764  
- Los Angeles Office -      Fax: 310 662 4767  
222 N. Sepulveda Blvd      Mobile: 310 704 7079  
Suite 2000  
El Segundo, CA, 90245  
Email: [arnold.alderman@anagenesis-inc.com](mailto:arnold.alderman@anagenesis-inc.com)**

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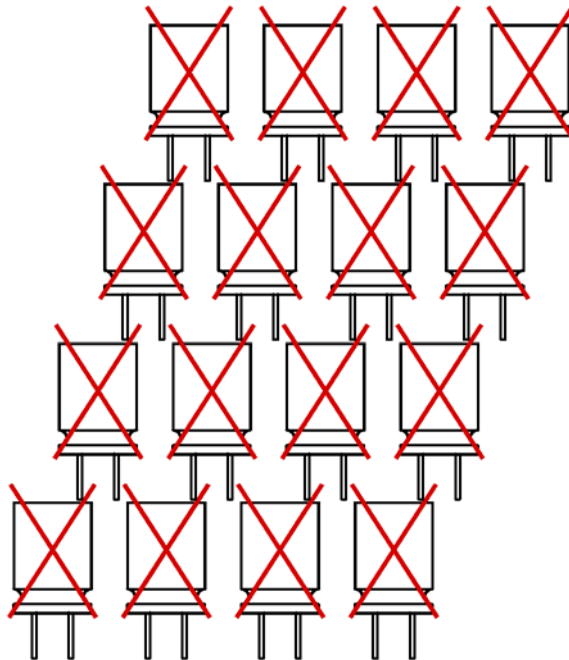
## 1.0 Introduction

The switched current power converter, or “SCPC”, provides a very fast current and voltage control suitable for high di/dt without the usual bulk capacitors. With supplemental switched charge circuits, the SCPC provides very rapid and precise step voltage changes, even with simultaneous load changes or a load dump.

This presentation summarizes the results of several SPIC model and simulations, then presents the full details of the SPICE models and SPICE oscillographs.

The presentation starts with a brief description of the SCPC, with some theory. A much more detailed write-up is "Switched Current Power Converters", Edward Herbert Revised March 11, 2006. [Http://eherbert.com/Scpc7.pdf](http://eherbert.com/Scpc7.pdf).

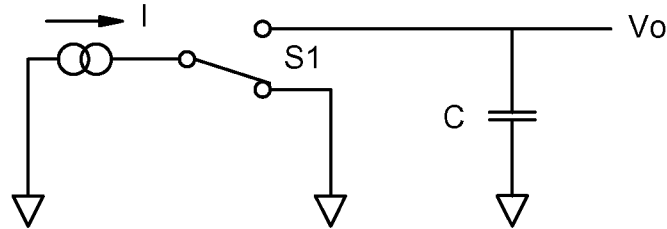
The SPICE models were done using Intusoft ICAP/4.



**Figure 1.1.** Because of its very fast response, the SCPC does not use bulk capacitors.

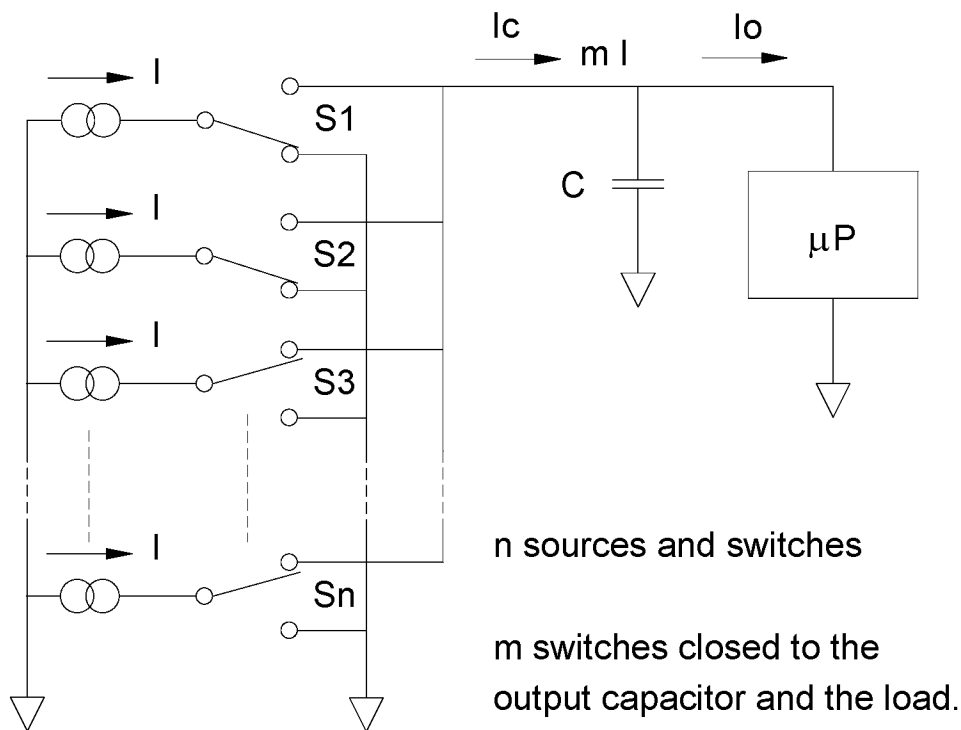
## 2.0. Switched Current Control:

The control strategy of the switched current power converter is very simple: A current is established, and then it is switched to the output capacitor and the load as required.



**Figure 2.1.** There is no faster control method than turning a switch on and off.

For a higher current load, it is preferred to divide the current into a number of parallel paths. It is tempting to compare a SCPC with a multi-phase buck converter, but that circuit has a very complicated control. A better analogy is a totem-pole buffer driver circuit.



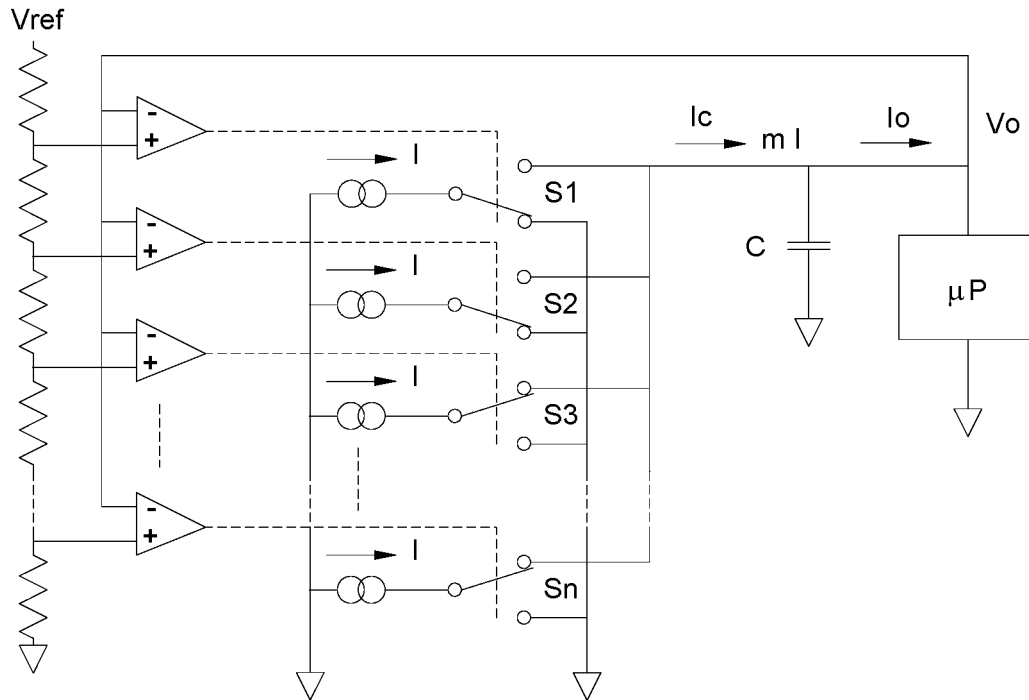
**Figure 2.2.** For currents that are less than full load, one or more of the switches is pulse width modulated so that the average current is correct.

There are several designs for the current sources, and there are several designs for controlling the current. All have in common the digital interface to the MOSFET drivers, so the current source design and the control design are very independent, and the common interface allows great flexibility in circuit applications, mixing and matching easily for various power sources and various loads.

### 3.0 Measurement:

#### 3.1. Flash Analog to Digital Converter:

A fast current modulator needs a fast measurement and control system, and there probably is no faster measurement than a flash analog to digital converter. A number of comparators have as their references the nodes of a resistor ladder network.



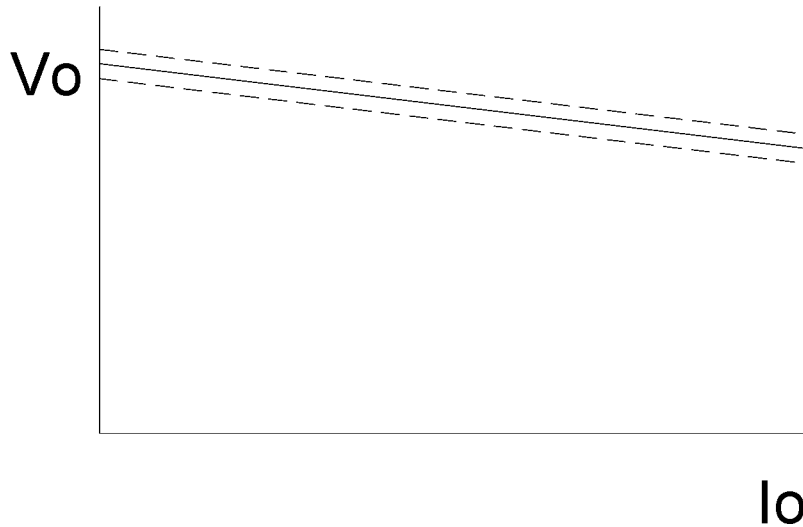
**Figure 3.1.** The outputs of the comparators of a flash analog to digital converter directly control the current switches, which are totem pole MOSFETs. This is a very fast control.

The delay time from sensing a change of state to a change in output is the propagation time of the comparators and the switching time of the MOSFETs with their drivers, which is tens of nanoseconds.

The comparators directly control the current switches of the switched current power converter. The characteristic of a power converter with such a control has a decreasing voltage with increasing current, which is what is usually specified for a processor power supply. For a simple system, no additional control or compensation is required. The accuracy is the accuracy of the voltage reference  $V_{ref}$ , the resistor ladder network and the offset voltages of the comparators. There are no other amplifiers, with their accuracy, bandwidth and slew rate limitations.

If there are several capacitors with significant parasitic impedance between them, using the output voltage as the control input requires a compensation network for stability, which slows the response significantly. This problem is avoided if total charge measurement is used, as explained below.

This presentation and the SPICE simulation are based upon a design with a fixed voltage reference. For specialized applications, the voltage reference may be replaced with an analog input or a digital VID with a d-a converter, so that the output voltage can be varied in response to an external signal or VID. There may be an outer voltage loop, for a fixed output voltage or for remote sense. Because the current control loop is extremely fast, a very high bandwidth voltage control can be implemented.



**Figure 3.2.** The output characteristics have a decreasing voltage with increasing current, just as is specified for many processors. The output impedance of the SCPC typically is  $0.5 \text{ m}\Omega$ .

Because the nodes of the resistor ladder network are at successively lower voltages, the output characteristics have a decreasing voltage with increasing current, as shown in figure 2.3. By dividing the voltage droop by the current, the output impedance is defined. Many processors specify a power source with a decreasing voltage with increased current. The output impedance of the SCPC typically is  $0.5 \text{ m}\Omega$ .

The present specifications for voltage droop, such as Intel® VR 10.2, accommodate the best capabilities of present power converters. It is a desired feature for processors. It stands to reason that a higher voltage at idle conditions does nothing beneficial for the operation of the processor, but it does substantially increase the power consumed by the leakage currents when the processor is not busy. These losses increase as a factor of voltage squared, so a lower output impedance is very beneficial.

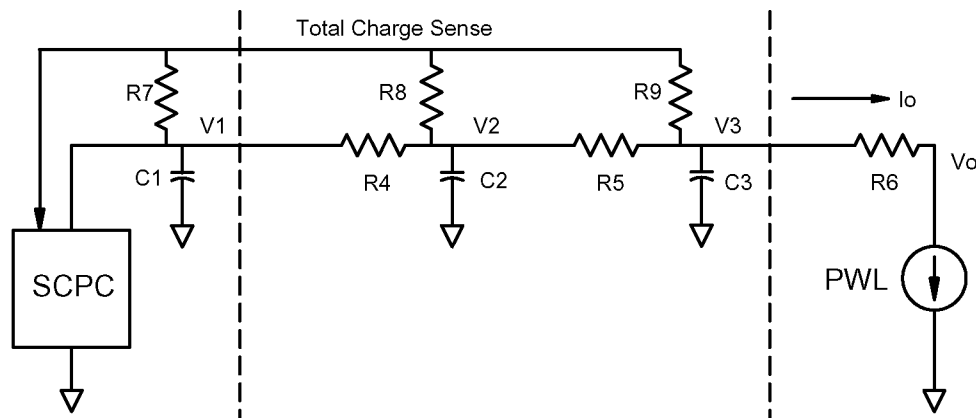
A practical resistor ladder network is somewhat more complex than the one shown in figure 2.1, because hysteresis must be added to limit the switch cycle frequency. See ["Switched Current Power Converters"](#), Section 5.0, for more information on hysteresis, output impedance, timing and capacitance size.

### 3.2. Total Charge Measurement:

A total charge measurement with a flash analog to digital converter provides an extremely fast and stable control. It is extremely simple, thus inexpensive, and only the resistors of the ladder network and its voltage reference need be particularly accurate. It is unconditionally stable at any frequency and has a phase margin of nearly 180 degrees.

For a high-speed control, current measurement is not practical. Not only are current measurement circuits very complex, they are also hopelessly slow. Voltage measurement at the output is not suitable either, as it may take a long time to settle down, far longer than is useable for control purposes for a fast power converter.

The solution is to measure the total charge of the capacitors in the power distribution system. This is an exquisitely sensitive measurement of current change, and it is immune to the voltage transients and ripple within the power distribution path.



**Figure 3.3.** The total charge on several capacitors can be measured with a resistor connected to each capacitor or group of capacitors. The *conductivity* of the resistor is proportional to the capacitance with which it is associated.



## 4.0. Voltage Control for SCPCs:

### 4.1 Voltage Control by Varying the VID.

With reference to figure 3.1, the output voltage  $V_o$  of a switched charge power converter can be changed by changing the reference voltage,  $V_{ref}$ . The reference may be an analog input signal or it may be a VID with a d-a converter. If the VID is changed, the output voltage will follow if the change is not too fast. In the SPICE model used for this presentation, with a 35 A load, a reasonable  $dv/dt$  limit is about 90 mV/ $\mu$ s increasing, and about half that decreasing.

The  $dv/dt$  limitation is due to the current available to charge the output capacitors, and the size of the output capacitance. For the example of a SCPC with 100 A rated current, if the load is 35 A, there is just 65 A available to charge the capacitor to a higher voltage. Reducing the voltage is a worse situation, as the SCPC usually cannot sink current, so decreasing the voltage relies upon the load absorbing charge from the output capacitor. A smaller output capacitance will allow a faster  $dv/dt$  by VID ramping. SPICE simulations and the models used are shown in Appendix 4.

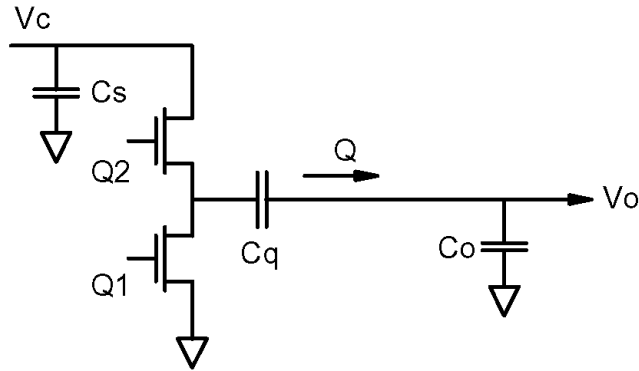
### 4.2. Voltage Control by Switched Charge.

The switched charge circuit operates entirely separately from the switched current circuits, and can be added as an accessory with no other hardware change. Only the VID input and the connection to the output capacitors are common. A separate connector for a switched charge module can be next to the SCPC module, and the power system can be enhanced by plugging in the switched charge module with no other hardware changes. There are several choices for implementing a switched charge voltage control. The same interchangeability is true for any of them, so any “flavor” of switched charge circuit can be used. The user can “plug and play” as desired.

The voltage  $V$  on a capacitor is given by the charge  $Q$  times the capacitance  $C$ . If the charge is changed, the voltage will change proportionately. If a precise charge is added to, or removed from, a capacitor, its voltage will step by a precise amount, and this can be achieved very quickly with solid state switching.

Figure 4.1 shows a basic switched charge circuit, consisting of a totem pole driver and a capacitor  $C_q$ . When the driver goes high, as precise charge is transferred to the output capacitor  $C_o$ , and when it goes low, a precise charge is removed, causing a precise and very fast output voltage step.

The switched charge circuit has no ability to regulate the output voltage, only to step it rapidly. Continued voltage control is done by the basic SCPC control, by controlling the current as explained above. Accordingly, the voltage reference VID must simultaneously step by the same amount so that the ongoing voltage regulation is at the new level.



**Figure 4.1.** When the switch changes state, a fixed charge  $Q$  is added to or removed from the output capacitor  $C_o$ , resulting in a fixed step in the output voltage, up or down.

A stepped charge circuit may provide one step, for power up, or a few steps, for specific discrete voltage changes, or it may be a binary sequence. With five binary stages, any of 32 discrete voltage steps may be commanded, in any combination, from any level to any other level, extremely rapidly. SPICE models are shown in Appendix 2.

## 4.0. SPICE Simulations:

SPICE models were done for a number of SCPC variations and simulated conditions. In the appendices of this presentation are the complete SPICE model as well as simulation results using the SPICE oscillograph.

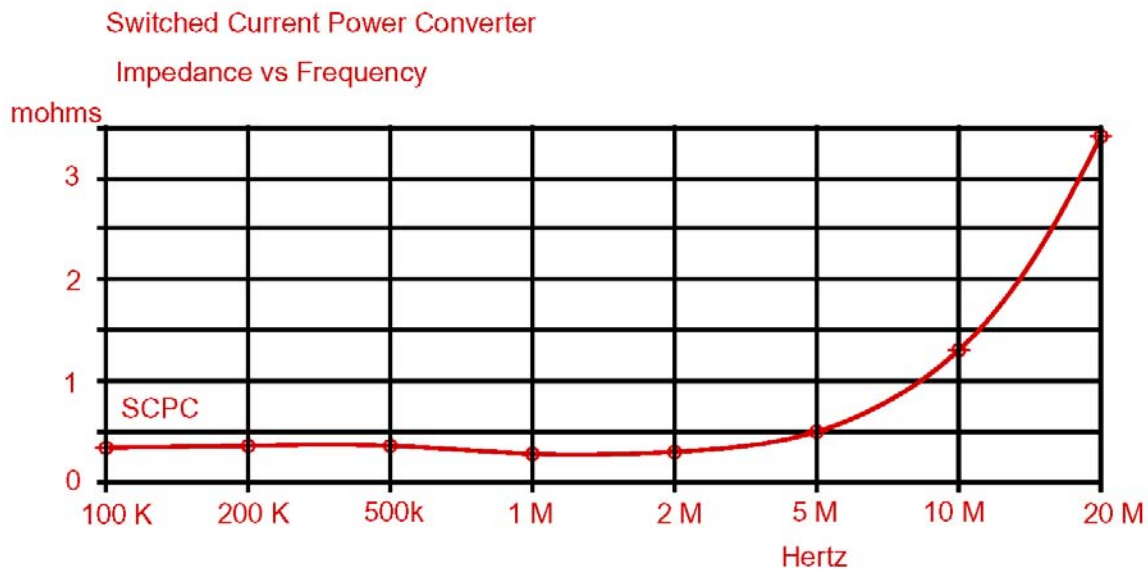
The simulation used a very conservative model for the output load, using representative parasitic impedances from an Intel® application note, “Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.2”, Intel® document number 306760-001 (March 2005). The SCPC control very fast, fast enough so that the large bulk capacitors are not needed, and they have been left out of the SPICE model.

The SCPC with total charge control largely mitigates the series parasitic impedances between the VRM and the decoupling capacitors. An additional parasitic inductance and resistance was added to the SPICE model, to show off this feature and to simulate the SCPC being located in a separate module that is not optimally close to the decoupling capacitors and the processor. The decoupling MLCC capacitors should be on the motherboard near the processor, and that is assumed in the SPICE model.

### 4.1. Summary:

#### 4.1.1. Output impedance:

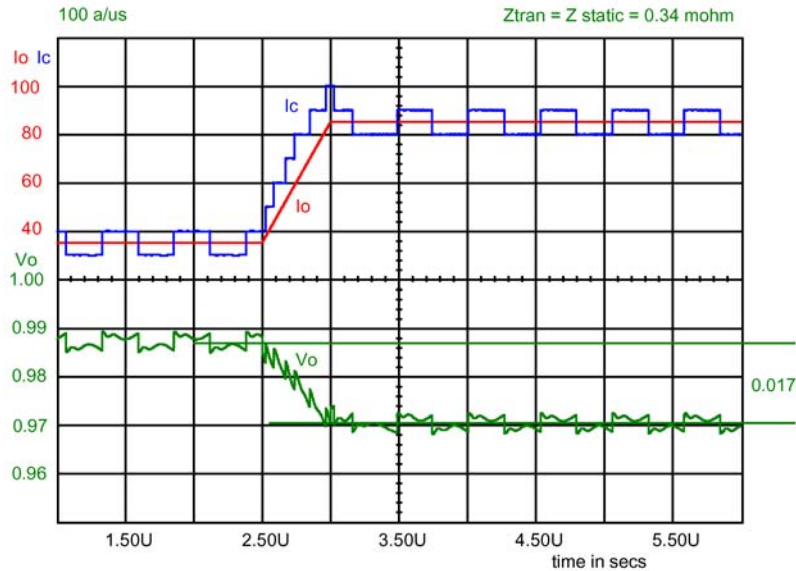
To determine the output impedance at different frequencies, a sine current load at the various frequencies was applied to the output of the SCPC. The sine current was a 50 A p-p sine wave on a 60 A dc, so that the current varied from 35 to 85 A. The resulting voltage change was measured, and the impedance was calculated as  $dv/dI$ .



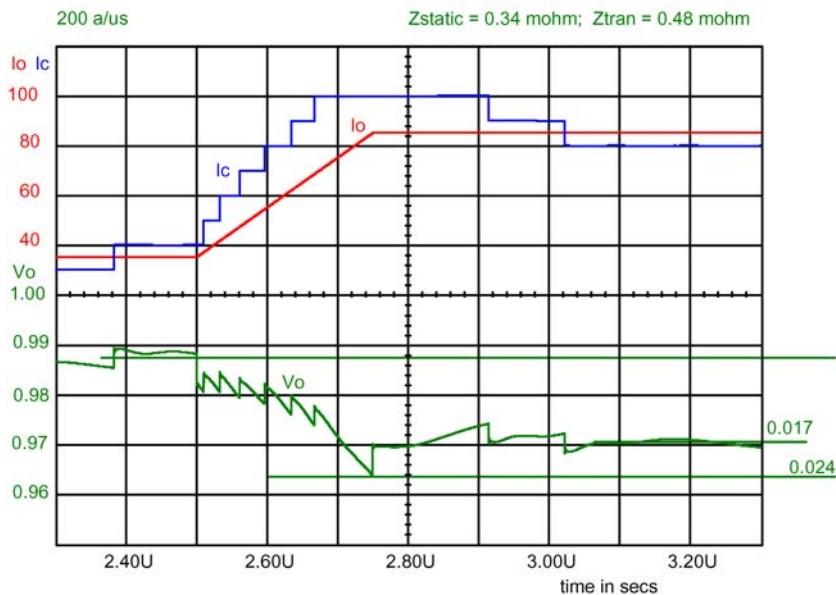
**Figure 4.1.** The impedance versus frequency of the SCPC for a family of SPICE simulations using conservative motherboard and connector parasitic inductances.

### 4.1.2. Transient Response, Step Current:

Current transients from 35 A to 85 A with  $di/dt$  of 100 and 200 A/ $\mu$ s were modeled in SPICE, and the resulting graphs follow. Note that the voltage is controlled through the transient, with a very slight undershoot at the higher rate of change ( $di/dt$ ). Adding to the capacitance does not improve the  $di/dt$  at higher rates. The parasitic impedances must be reduced to step at a higher rate. This will be the topic of a future presentation.



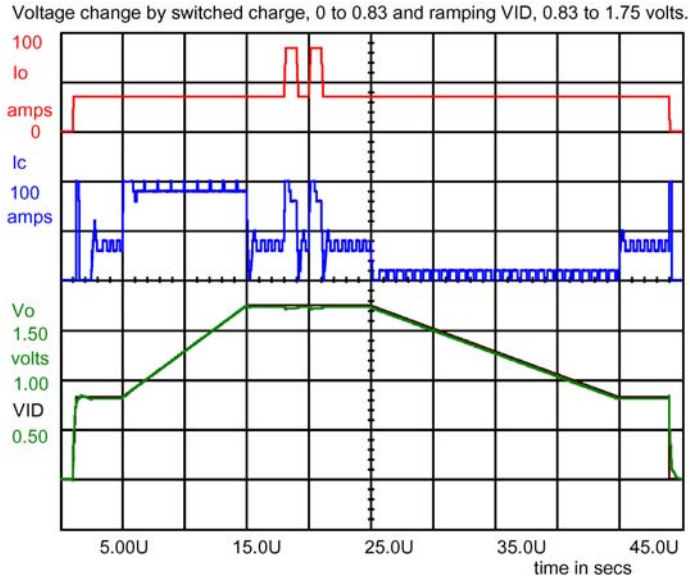
**Figure 4.2.** A spice simulation of 50 A step at 100 A/ $\mu$ s using conservative motherboard and connector parasitic inductances.



**Figure 4.3.** A spice simulation of 50 A step at 200 A/ $\mu$ s. The dynamic impedance is increasing, so this may be the practical limit for  $di/dt$  unless parasitic impedances can be reduced.

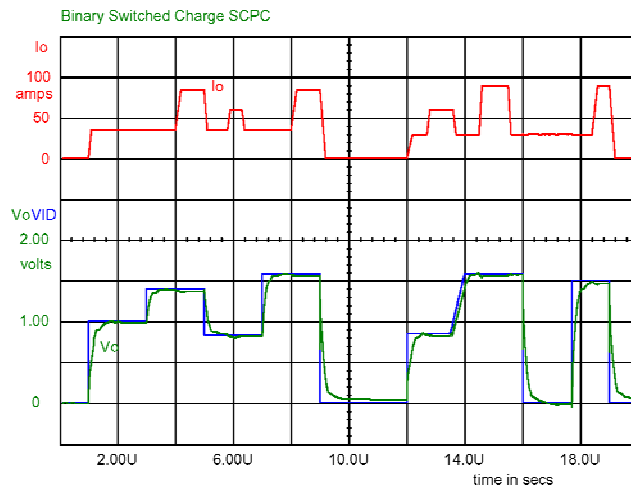
### 4.1.3. Transient Response, VID Command:

The ability of the SCPC to follow rapid changes in the VID was simulated for a number of scenarios, with and without switch charge circuits.



**Figure 4.4.** Voltage response to changes in VID, SCPC only.

The ability of the SCPC to track VID commands is limited by the current available. Increasing, it is the difference between the maximum current and the load current. Decreasing, it depends upon the ability of the load to sink current.



**Figure 4.5.** The voltage response is much faster using switched charge circuits.

With switched charge circuits added, the voltage can step very rapidly and precisely irrespective of the load. Note that at 9 us there is a simultaneous load dump and transition to 0 V.

## Appendix 1

### Switched Current SPICE Simulations:

#### A1.1. Schematic:

The schematic in figure A1.1 shows the SPICE schematic used for the transient and frequency response simulations. The load impedance network is based upon the equivalent circuit for the motherboard and socket from Intel Design Guidelines, Document Number 306760-001, “Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.2”, March 2005, The large bulk capacitors were left out, as the fast response of the switched current power converter makes them unnecessary.

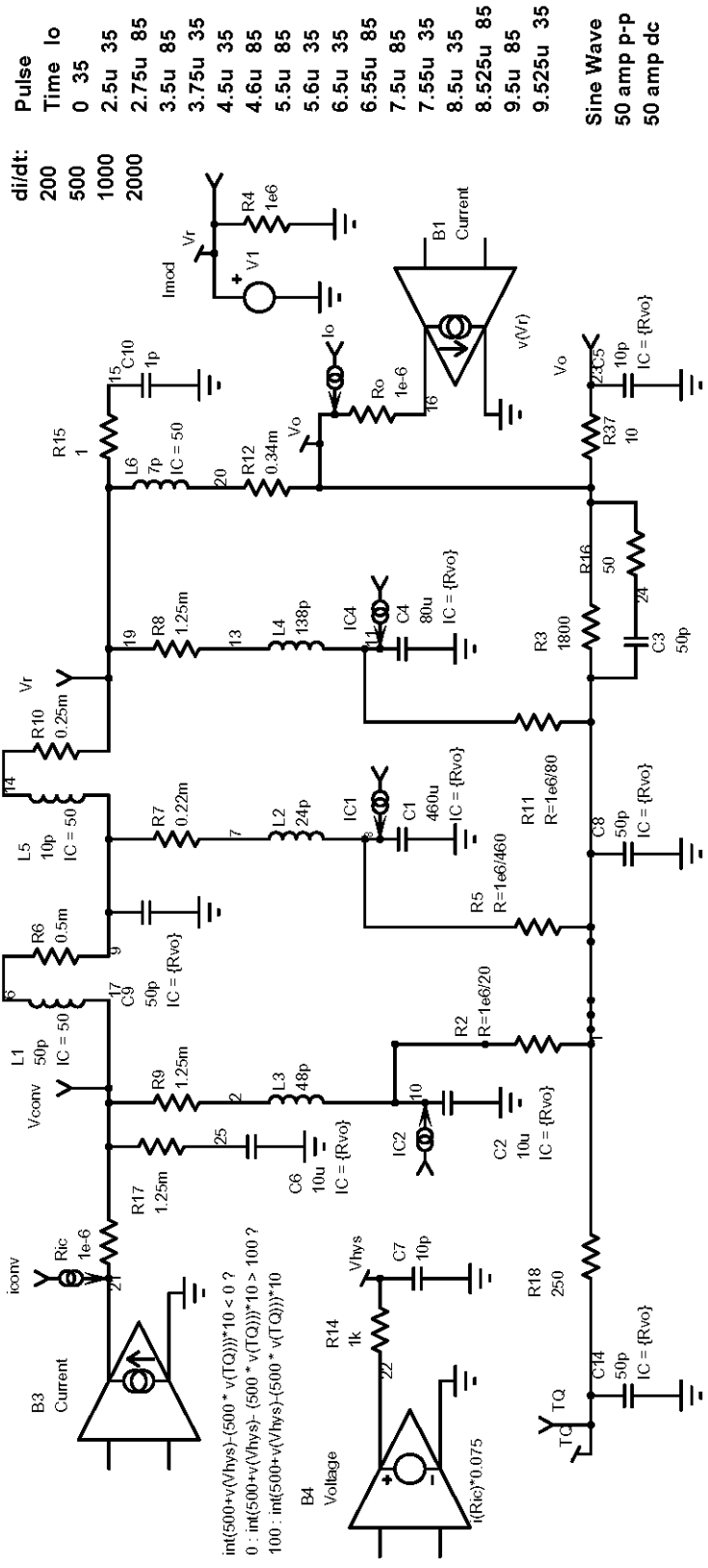
An additional parasitic inductance (L1) and resistance (R6) were added to simulate the case where the power converter is not optimally close to the power supply, though it is assumed that the bypass capacitors are optimally close to the processor on the motherboard. These were used to simulate a VRM connector, and to show off that the total charge measurement and control system largely mitigates its effects. Because the decoupling capacitors are to be on the motherboard, the impedances for the EVRD model were used.

Various odd components appear in the circuit, and are necessary for the SPICE simulation to run well. Some of these are mysterious, and serve as a caution that these simulations must be accepted for what they are, *simulations*.

In the SPICE model schematic of figure A1.1, the switch current power converter is the behavioral current source B3 at the left. The total charge measurement system is shown at the bottom, and the node “TQ” (for “total charge”) is the control input for the current control algorithm. The SPICE used is Intusoft ICAP/4. It is suggested that the reader duplicate the model and try the simulations.

The load is the behavioral current source B1, and its current is controlled by the programmed voltage source V1. The capacitor C9 was needed for the current source B1 to operate correctly. For the transient simulation, the current may be programmed as shown in the chart at the right. The transient simulation time is 6 microseconds, of which the first microsecond is not displayed, to allow for the initial conditions to settle. 50-A step pulses, from 35 to 85 A, are shown, with di/dt, respectively, of 100 and 200 A/ $\mu$ s. Faster simulations were run, but are not shown, as the higher di/dt is very dependant on the parasitic impedances, and this presentation is directed to the response of the SCPC with existing circuits.

The step current changes of 35 to 85 A at 100 and 200 A/ $\mu$ s were chosen to show the usual Intel step load test and to show the circuit at its practical limit, respectively. It is anticipated that faster response can be achieved with circuit board layout modifications, but that is the subject of a future presentation.



**Figure A1.1.** The SPICE model for the transient and frequency response measurements.

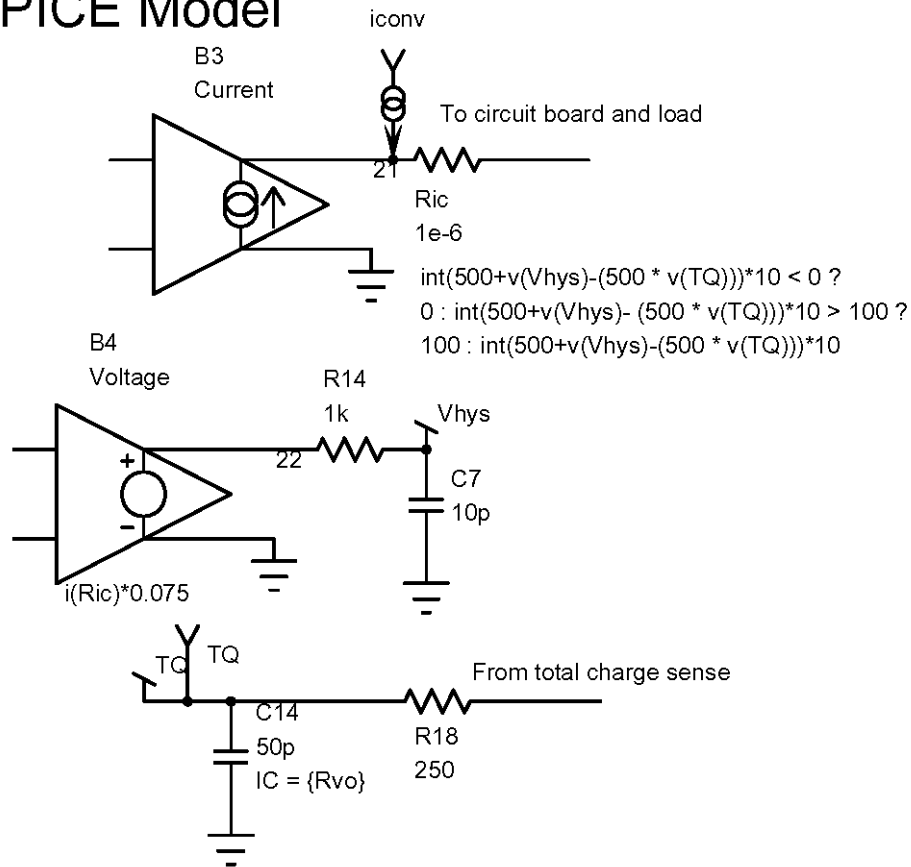
For the frequency response and impedance measurements, the voltage source V1 is programmed as a sine function with a 50 ampere offset and a 50 ampere peak to peak sine wave at the various frequencies. The impedance in the graph is the peak to peak voltage at the output  $V_o$  divided by 50, the peak to peak current  $I_o$ .

The details of the switched current power converter SPICE model is shown in figure A1.2. The algorithm for the behavioral current source B3 provides a current output as a function of the control input TQ. The fundamental equation is:

$$I_c = 5000 - 5000 * TQ$$

By using the “int” function, the decimal part of the expression is discarded. By applying this to an expression of one-tenth the value, then multiplying by ten, the output is constrained to be in discrete 10 A increments, as in a switched current power converter with ten channels of 10 A each. The expression is limited to values between 0 and 100 A. The Vhys function simulates hysteresis.

## Switched Current Power Converter SPICE Model



**Figure A1.2.** The SPICE model for the switched current power converter. The filters on the  $V_{hys}$  and TQ functions were necessary for the SPICE simulation to run well.

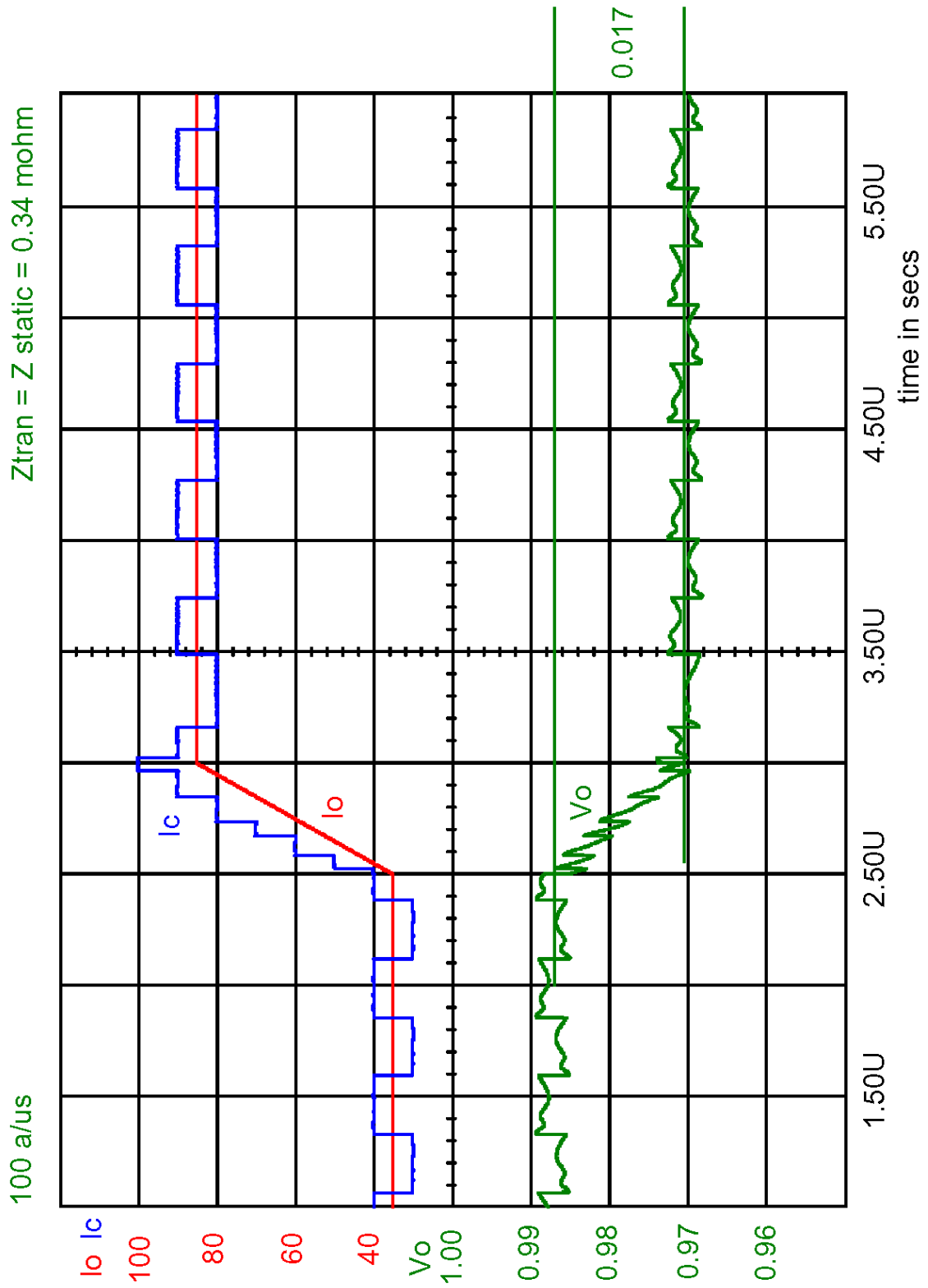


## A1.2. Transient Response Simulation:

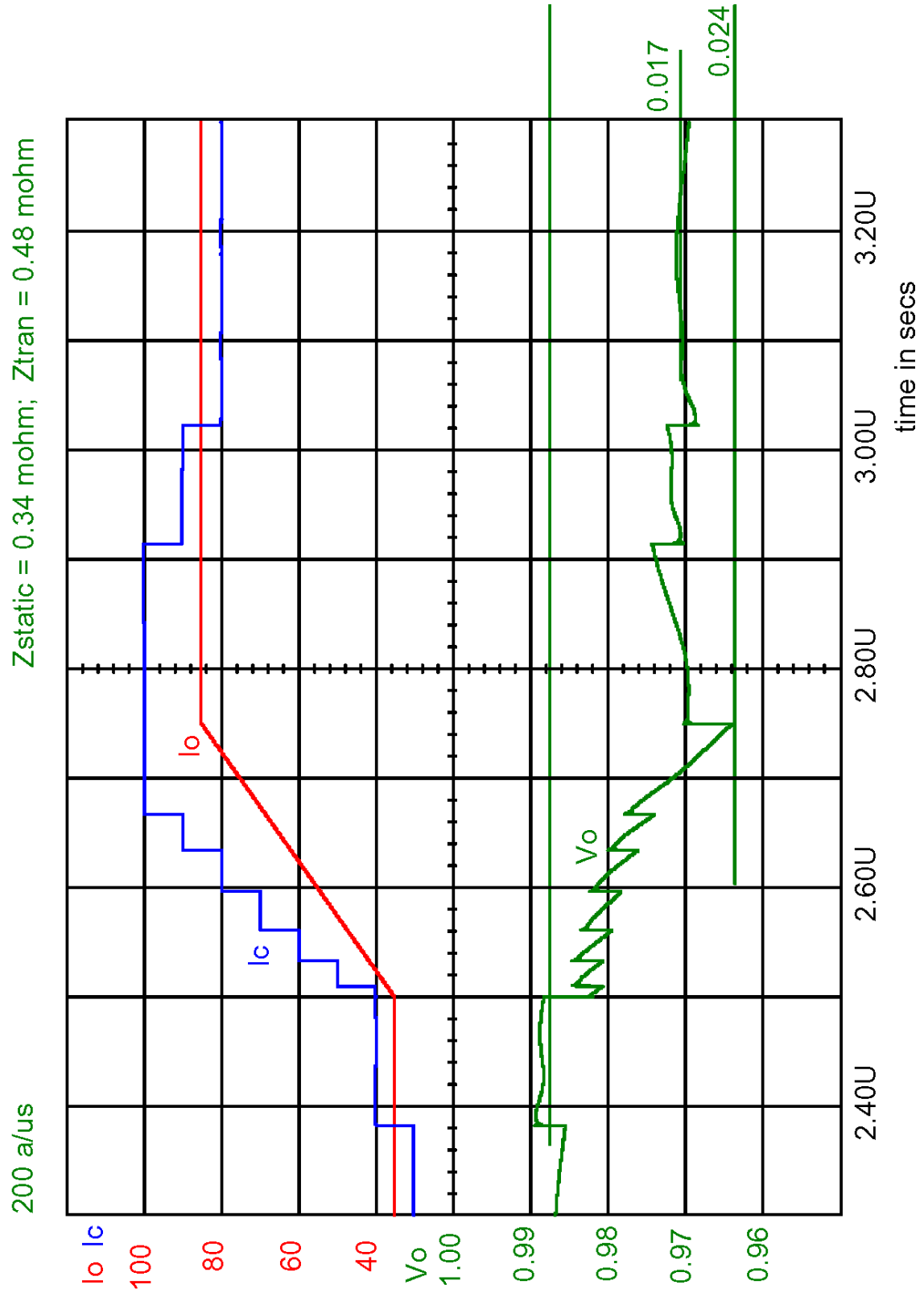
The figure A1.3 shows the SPICE simulation for the circuit described above for a 60 A step in current with a  $di/dt$  of 100 A/ $\mu$ s. This is one of the tests often cited in Intel specifications and application guides. It is easily handled by a switched current power converter as the transition is slow enough that the output voltage  $V_o$  is regulated through the transition.

Figure A1.4 shows the SPICE simulation at 200 A/ $\mu$ s. This may be about the practical  $di/dt$  limit to maintain regulation through the current ramp with the parasitic impedances of present circuit boards and capacitors. It can be seen that the current has saturated high, allowing an undershoot. The SPICE simulation does not simulate the propagation delay through the comparators and the MOSFET switches and their drivers. With a rise time of 250 ns, the delay will make the real undershoot greater. A 50 nsec delay may be practical, which would suggest that the undershoot might be 20 percent more.

Higher  $di/dt$  capability will depend upon a significant reduction in the parasitic impedances. This may be practical, but it is the subject of a future presentation.



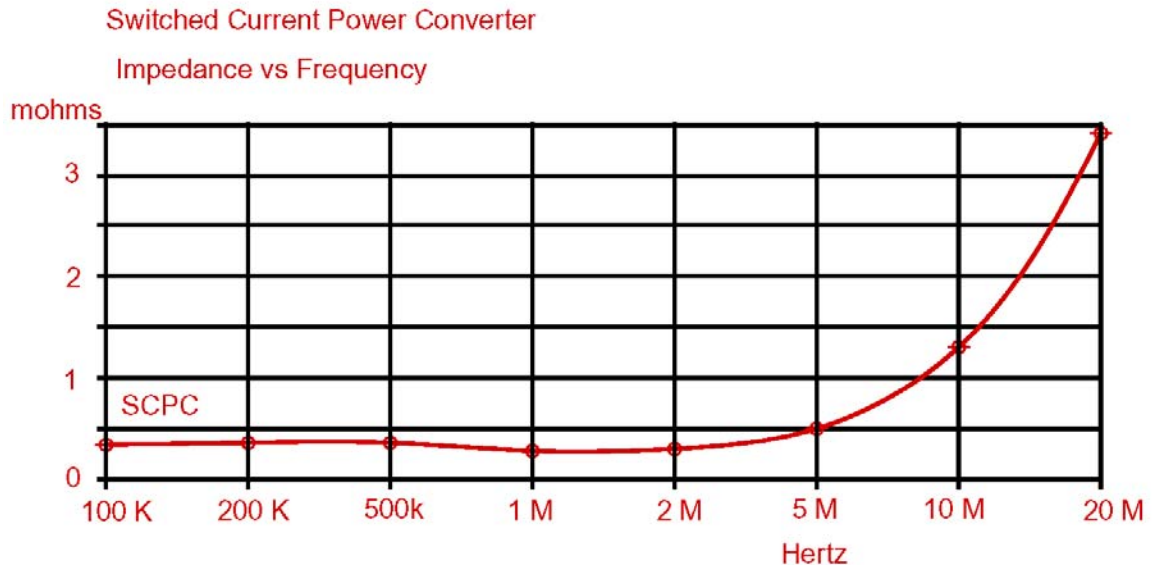
**Figure A1.3.** The static and dynamic impedance with a 50 A step current from 35 to 85 A at 100 A/ $\mu$ s are the same, 0.34 m $\Omega$ .



**Figure A1.4.** The static and dynamic impedance with a 50 A step current from 35 to 85 A at 200 A/ $\mu$ s.

### A1.3. Frequency Response Simulation:

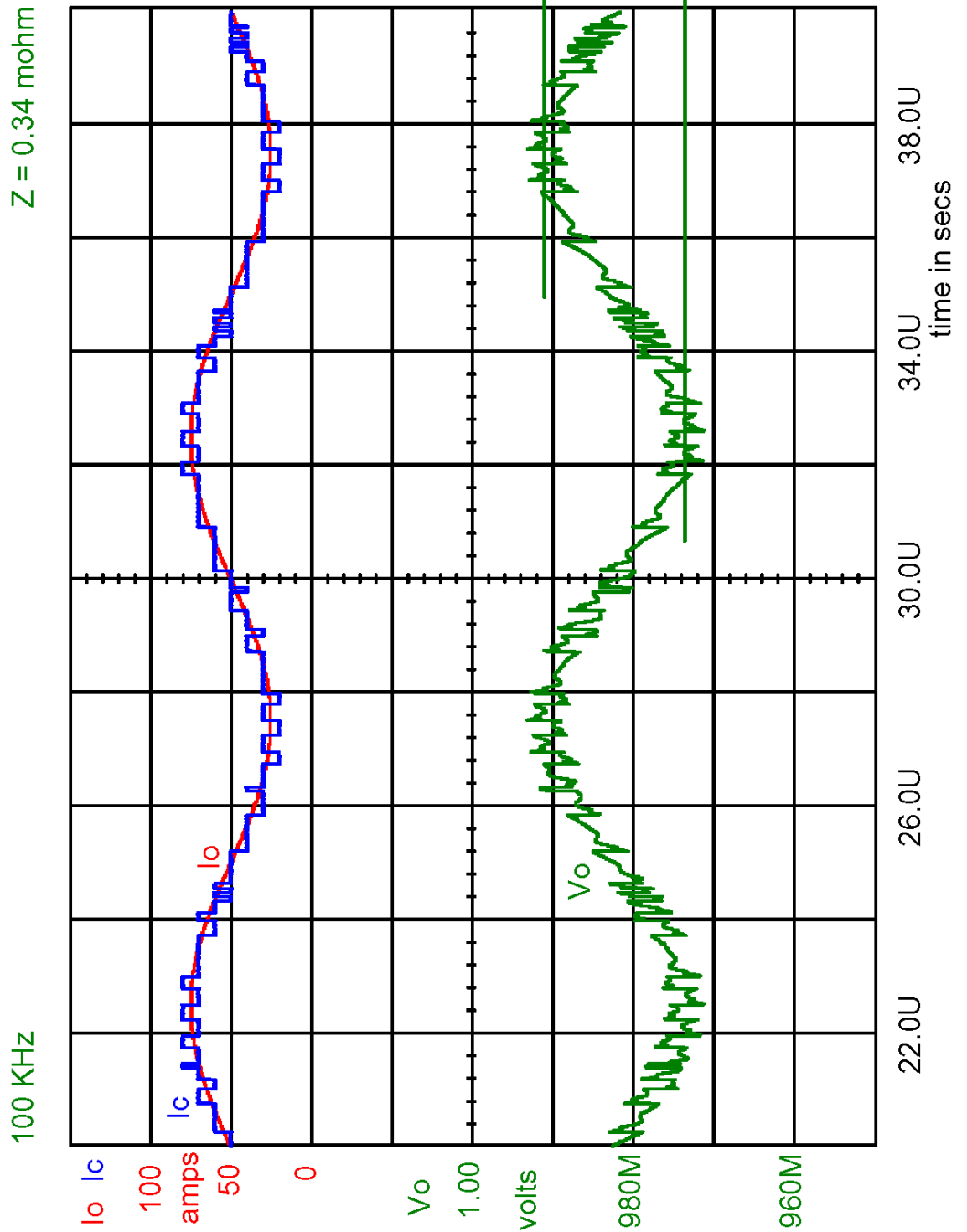
Figure A1.5 shows the output impedance  $Z$  versus frequency for SPICE model of the switched current power converter SCPC. The impedance is the peak-to-peak output ripple voltage divided by 50, the simulated ac peak-to-peak load current sine component.

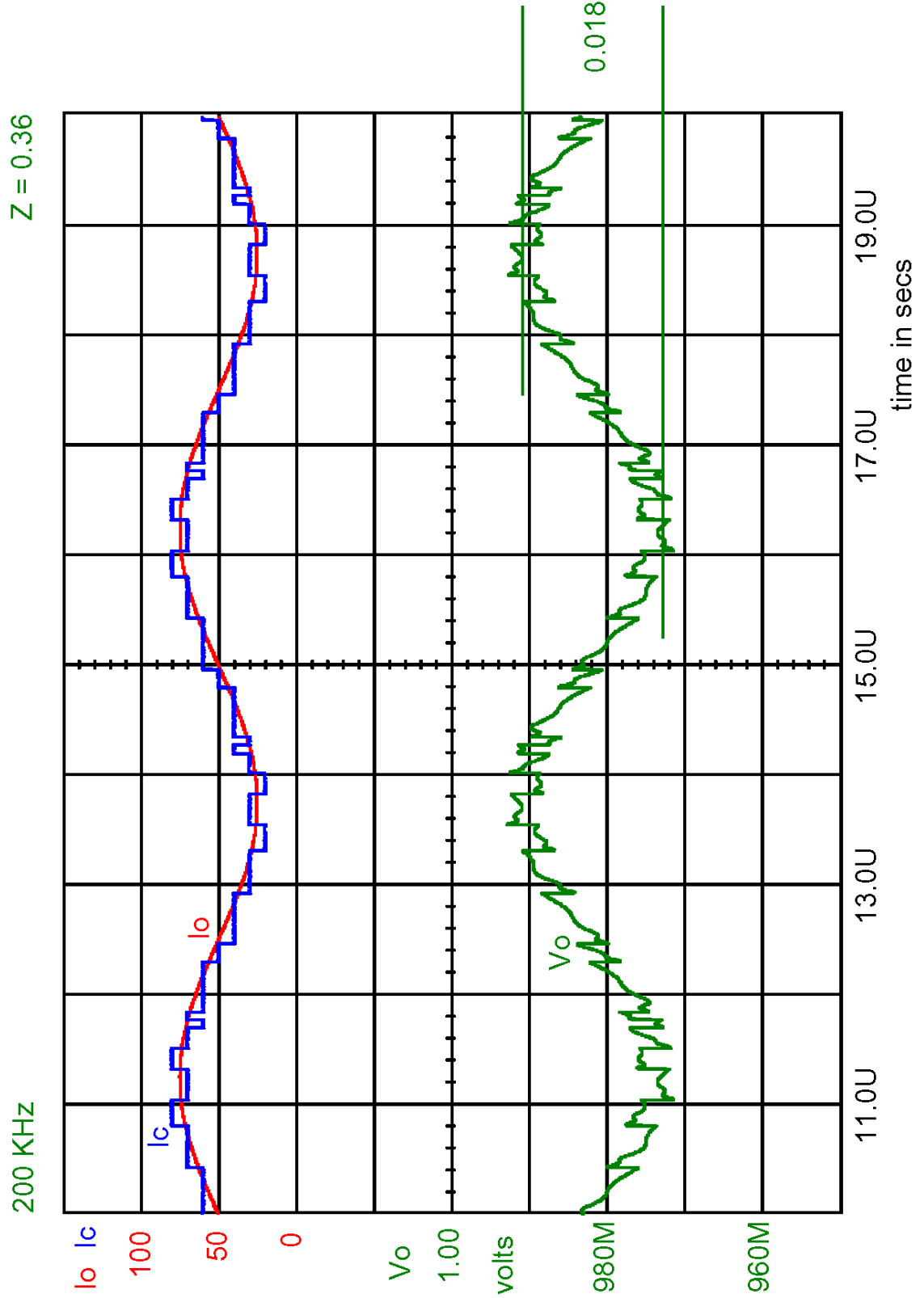


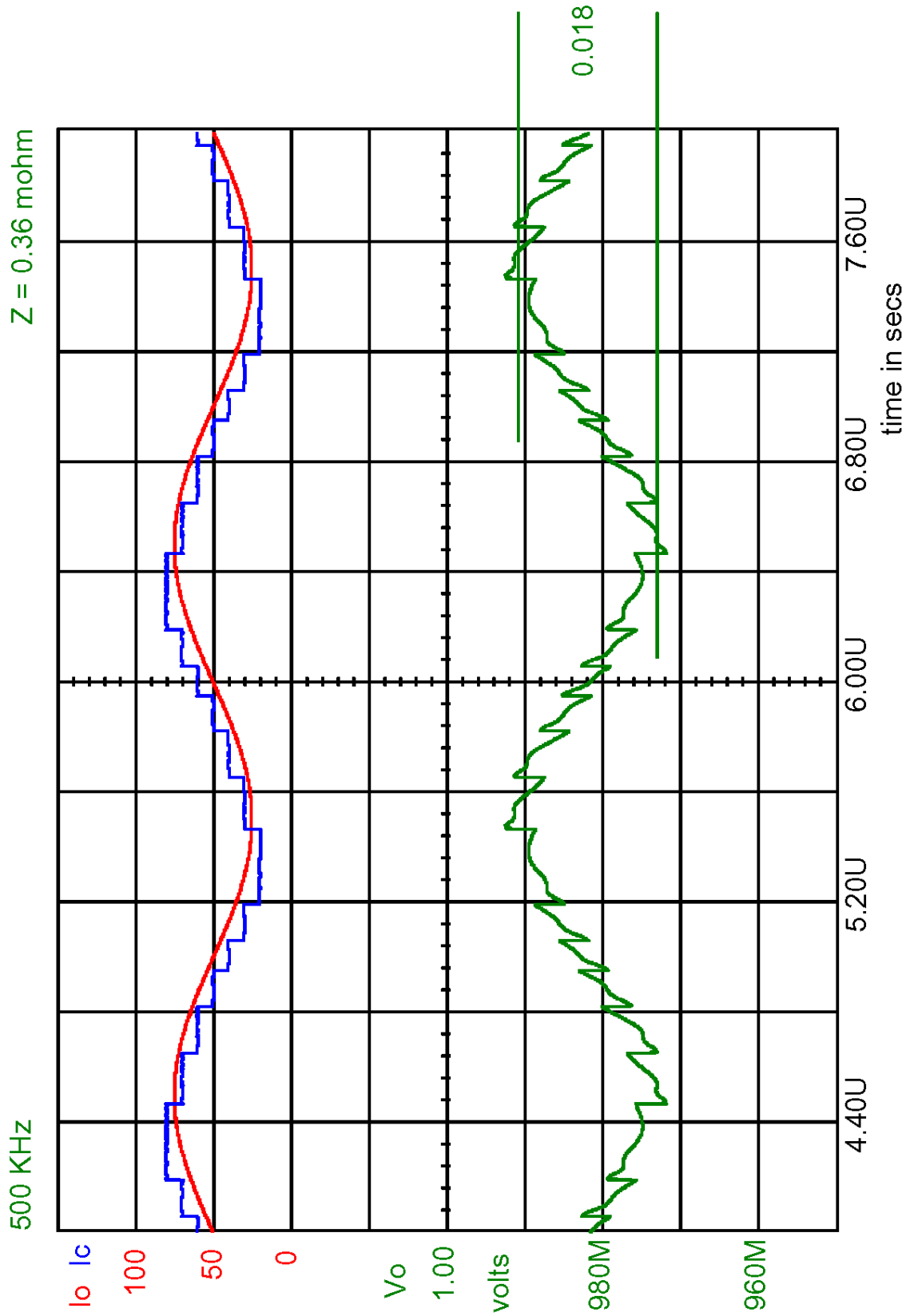
**Figure A1.5.** The output impedance of the switched current power converter SCPC is the peak to peak output voltage divided by 50, the peak to peak current load, at various frequency.

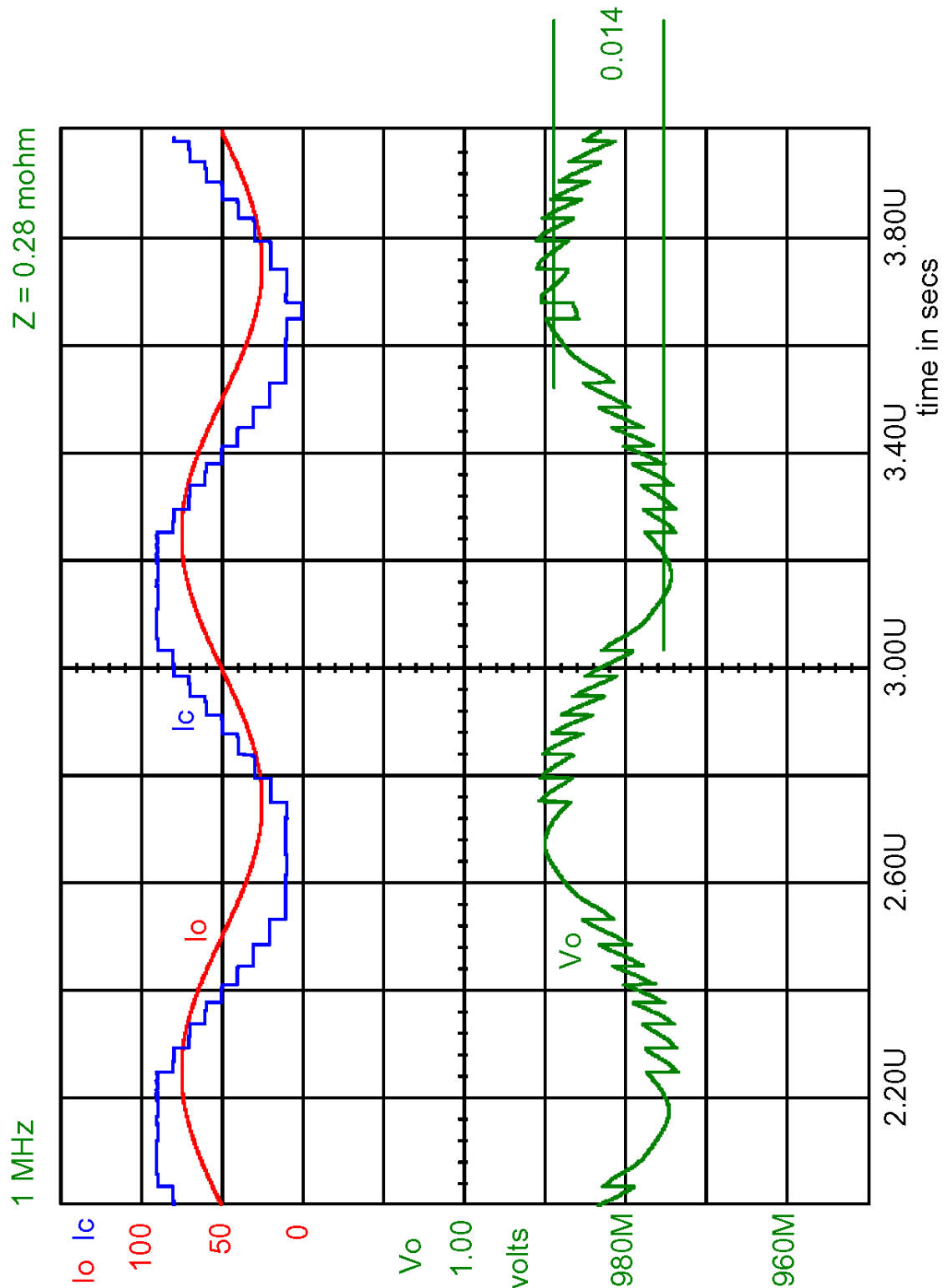
Following are eight graphs showing the raw simulation data for the impedance curve of figure A1.5. In each case, the simulation was run for several cycles before the graph was started, so initial conditions could settle. The ripple voltage is about 5 mV peak to peak.

In the SPICE models, the SCPC continues to respond throughout the test range of 100 kHz to 20 MHz, but above 5 MHz it has little effect on the output due to the series parasitic inductance. In a practical circuit, the delay time through the comparator and the switching time of the MOSFET and its driver will introduce a lag of tens of nsec. A lag of 50 nsec is a phase shift of 90 degrees at 5 MHz. A lead-lag network was used to improve the response at 5 MHz, admittedly by trial and error, in SPICE, but that is a very fast rate to be switching current, so steady state operation at that frequency is not advised. The advantage of the fast response is that control is maintained throughout step changes of current up to about 200 A/ $\mu$ s. It is not intended to be used as a high frequency sine generator.

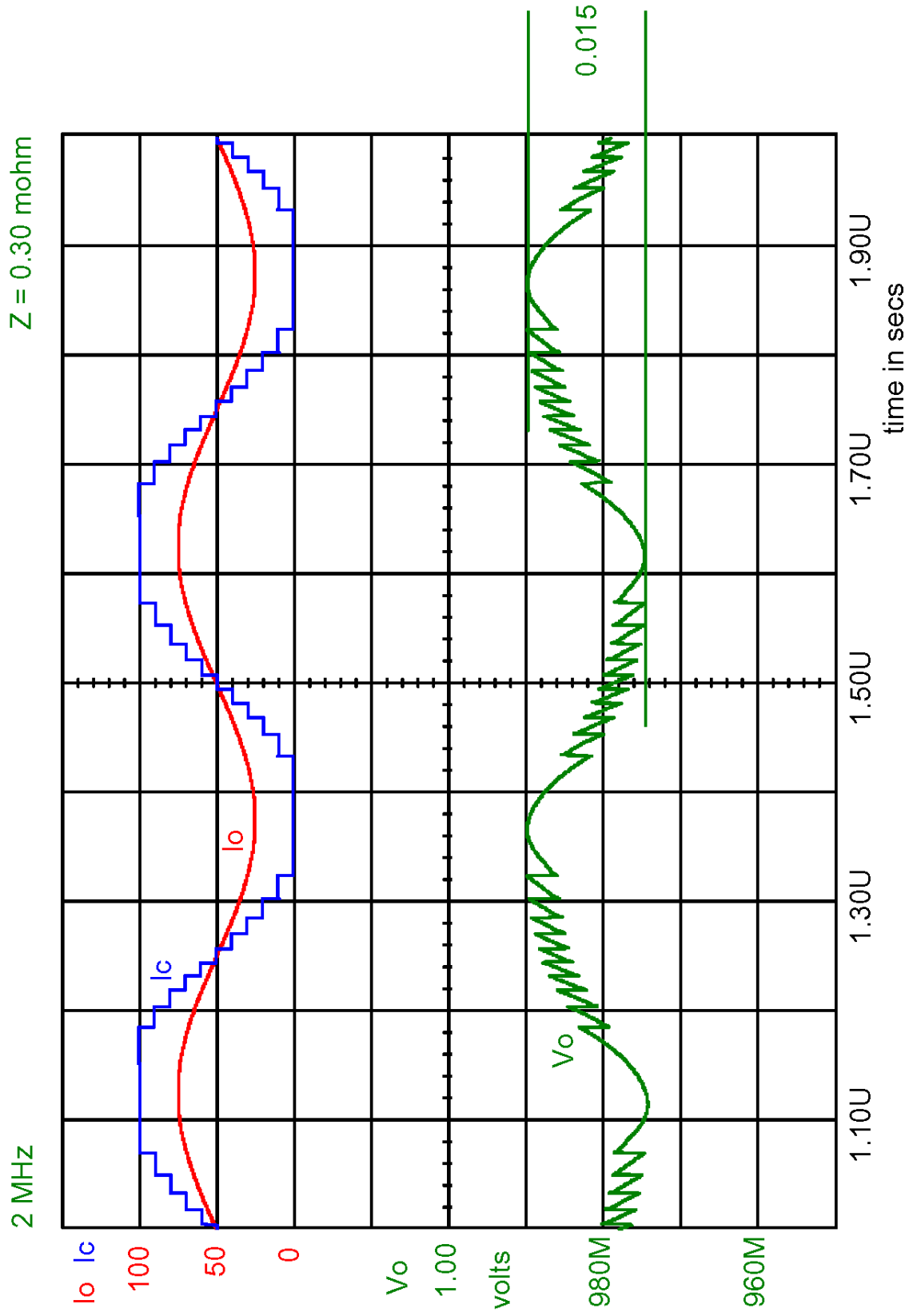


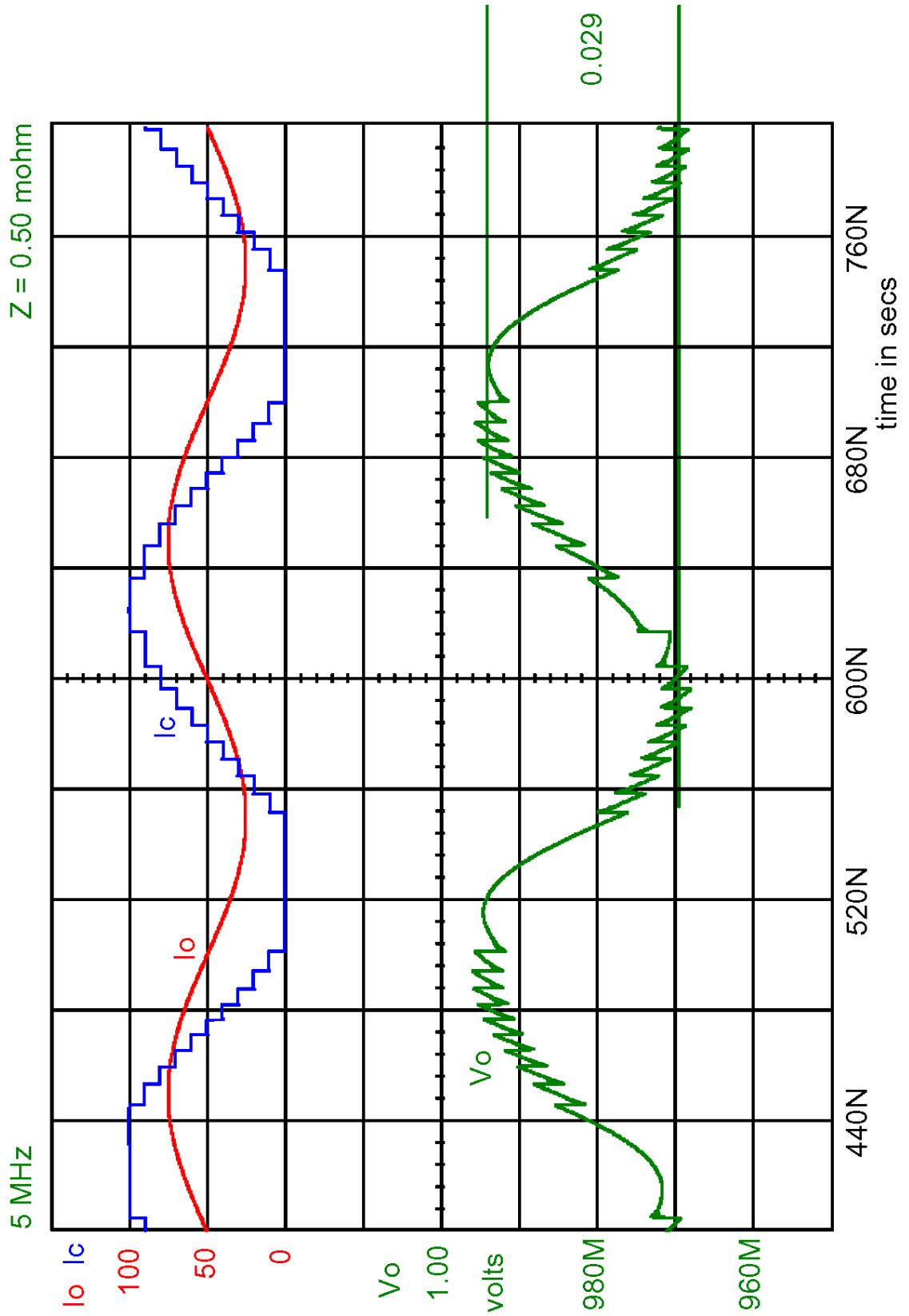


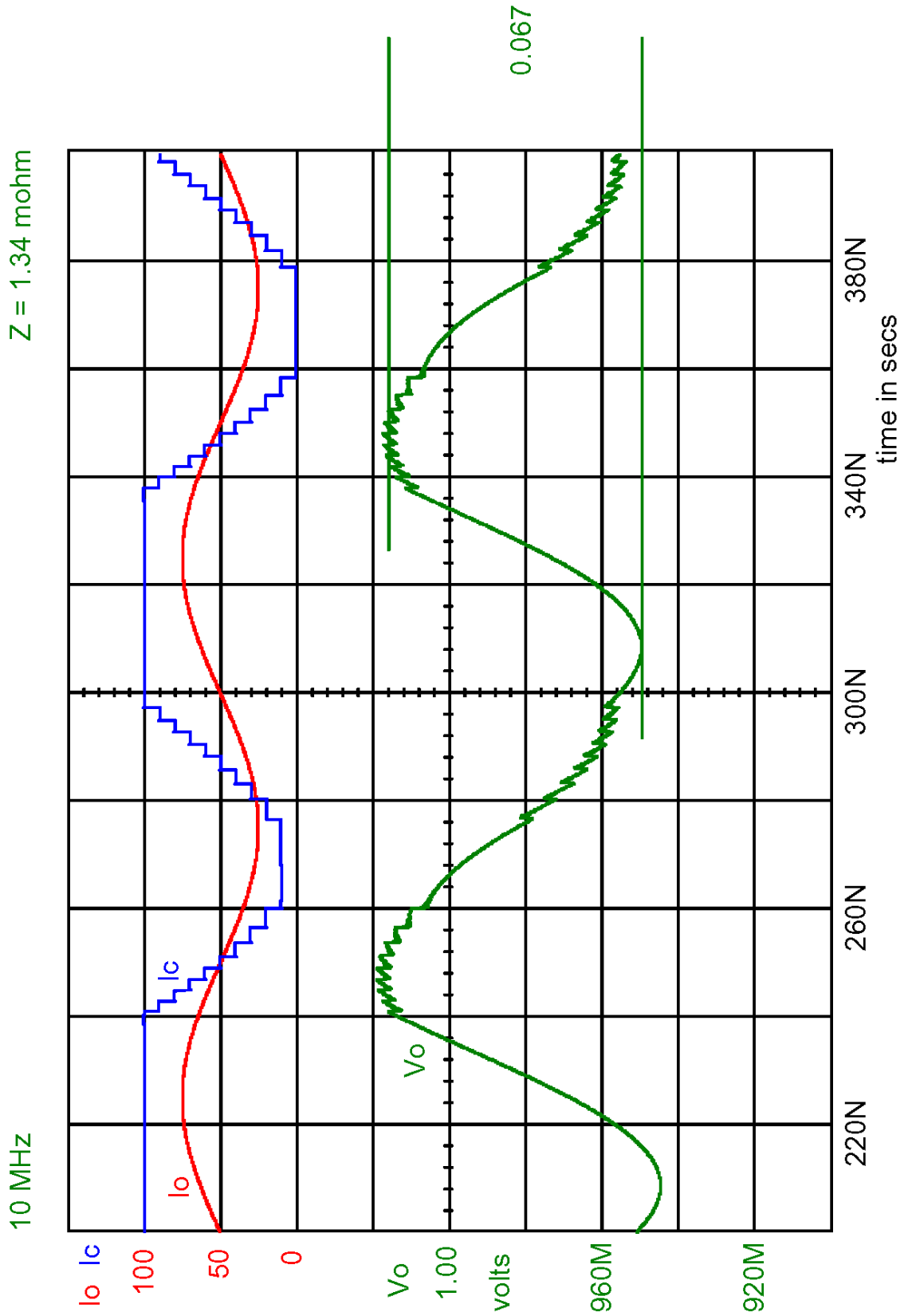


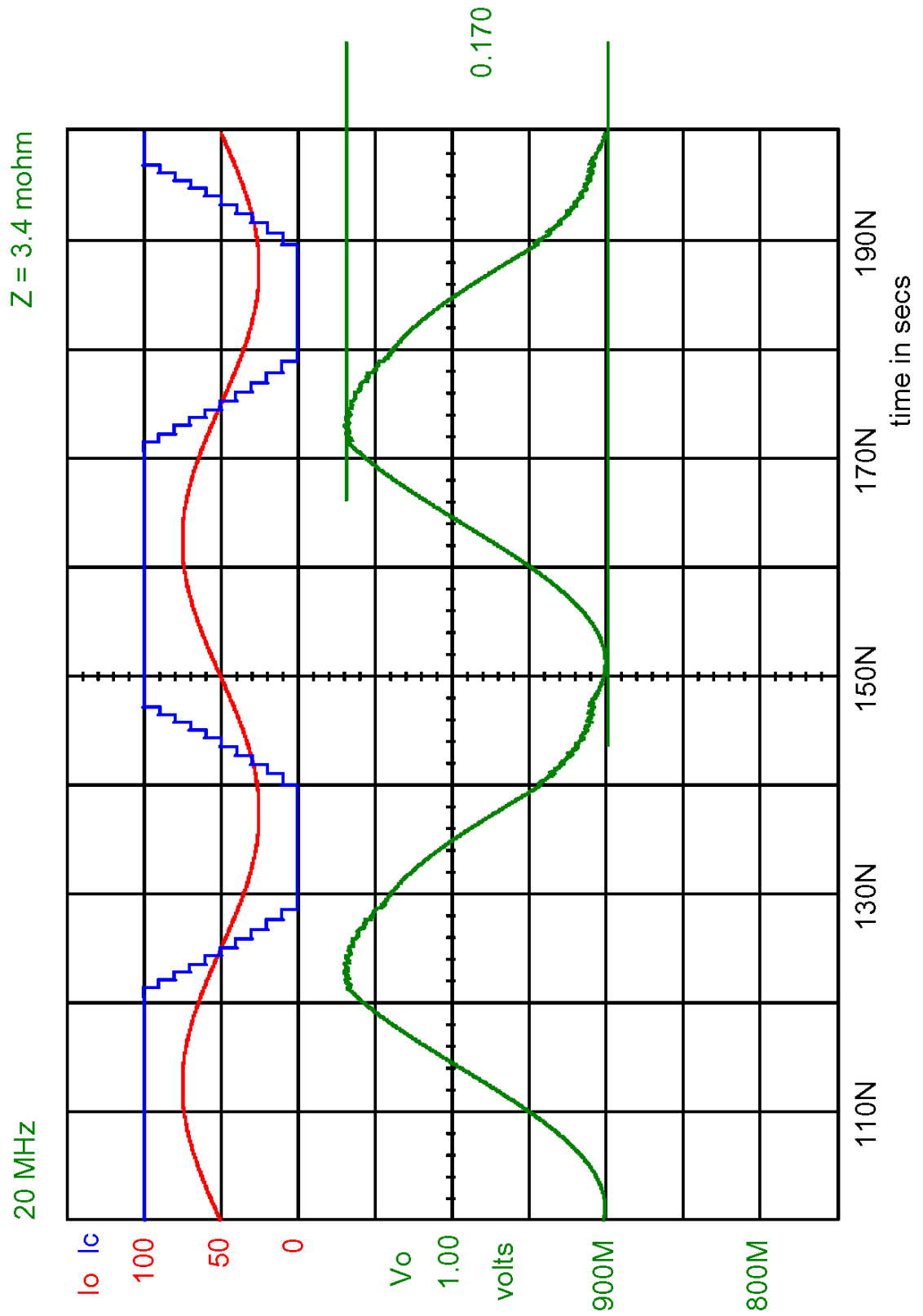












## Appendix 2

### Voltage Transition SPICE Simulations:

The voltage may be changed by changing the VID input. With the basic SCPC circuit, the VID may be ramped slowly (40 to 100 mV/ $\mu$ s, depending upon the load, for the SPICE model used).

For a faster response, the SCPC may be augmented with a switched charge circuit. The switched charge circuit is completely independent of the SCPC, and can be added as an accessory with no other hardware change other than plugging it in. There are a number of ways to design a switched charge circuit, as described below, and they can be interchanged at will by the end user, with no hardware change other than just plugging one or another of them into a parallel connector.

#### A2.1. Voltage Change by Ramping VID:

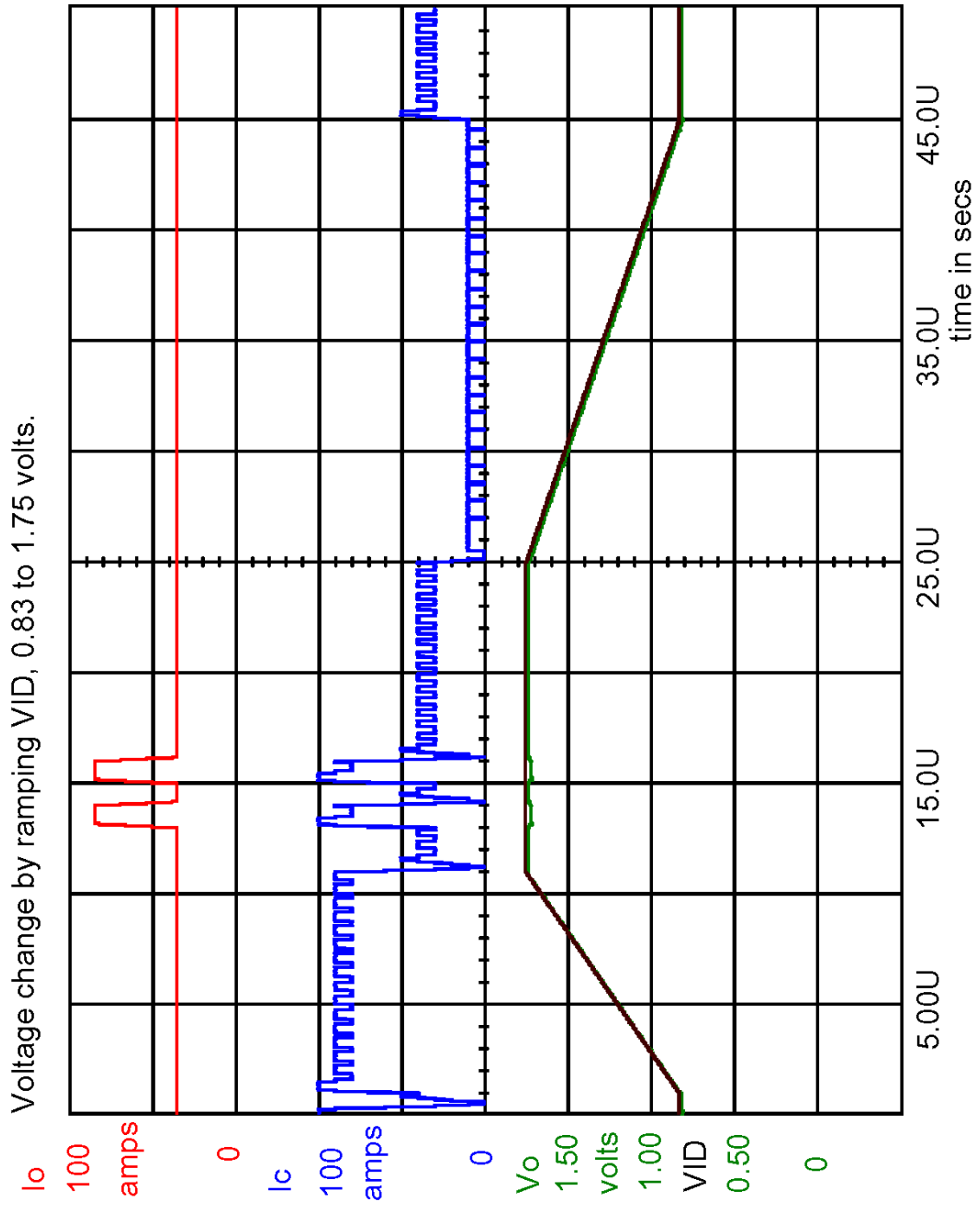
A very simple way to vary the output voltage of a switched charge power converter is to vary the reference voltage on the resistor ladder network. This can be from an input analog signal, from a VID input through a d-a converter or from an amplifier in a feedback system.

While very simple, this method of voltage control is limited by the saturation current, high or low, of the switched current sources. The fastest scenario is to step change the voltage reference, allow the SCPC to saturate high or low, then have a “voltage good” signal when the circuit catches up and the voltage control is regained.

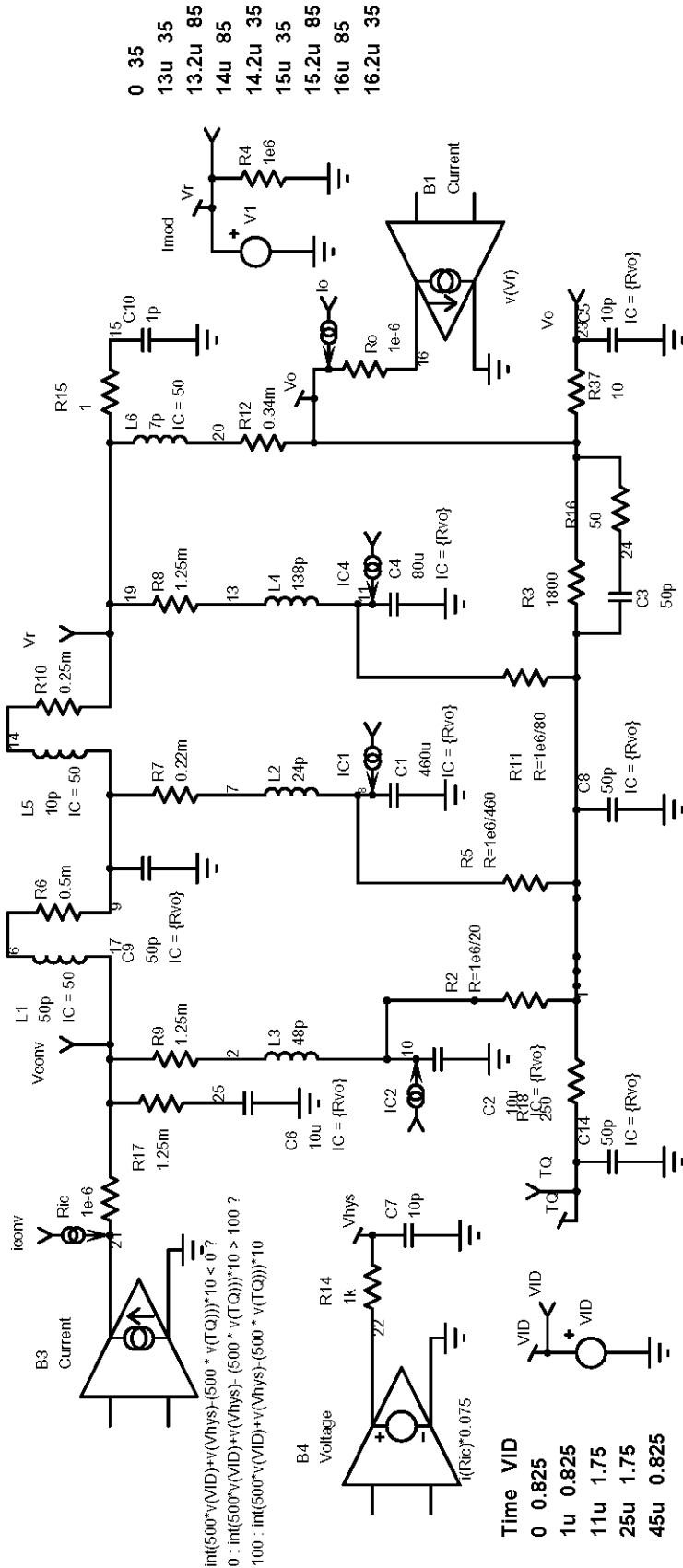
With a more slowly varying reference, the output voltage will track the VID faithfully. Presently, when a processor changes voltage to save power, the phase locked clock is resynchronized. Perhaps with a well-behaved power supply, the processor clock can be designed to slew, commanding the appropriate processor voltage as the clock rate varies.

Following is a SPICE simulation in which the VID input was ramped slowly enough so that the switched current source did not saturate. At the start of the simulation it is assumed that the voltage and current are stable at the minimum voltage and a 35 A output current. Because a 35 A load is used in the simulation, and the maximum current available is 100 A, the ramp up can be faster without saturating than the ramp down. The dv/dt limit for an increasing voltage ramp is about 90 mV/ $\mu$ s, and decreasing it is about half that. A smaller output capacitor would improve the dv/dt.

Following the SPICE simulation is the SPICE schematic. The reader is encouraged to do his own SPICE simulation and experiment with various scenarios. In the SPICE schematic, the VID input logic is incorporated into the current source B3 algorithm. The VID input is simulated by the programmed voltage source VID. The program sequence (time and voltage) are shown in the table next to the voltage source. A second voltage source V1 programs the simulated output current.



**Figure A2.1.** The output voltage is controlled by ramping VID.



## **A2.2. Voltage Change using Switched Charge and Ramped VID:**

A switched charge circuit is a totem pole output driving a capacitor. When the driver changes state, a fixed charge is added to or removed from the output capacitor(s). Adding or removing a fixed charge causes a fixed change in the output voltage, up or down. The voltage step is accurate, but the final output voltage depends upon the starting voltage, as only the step magnitude is controlled.

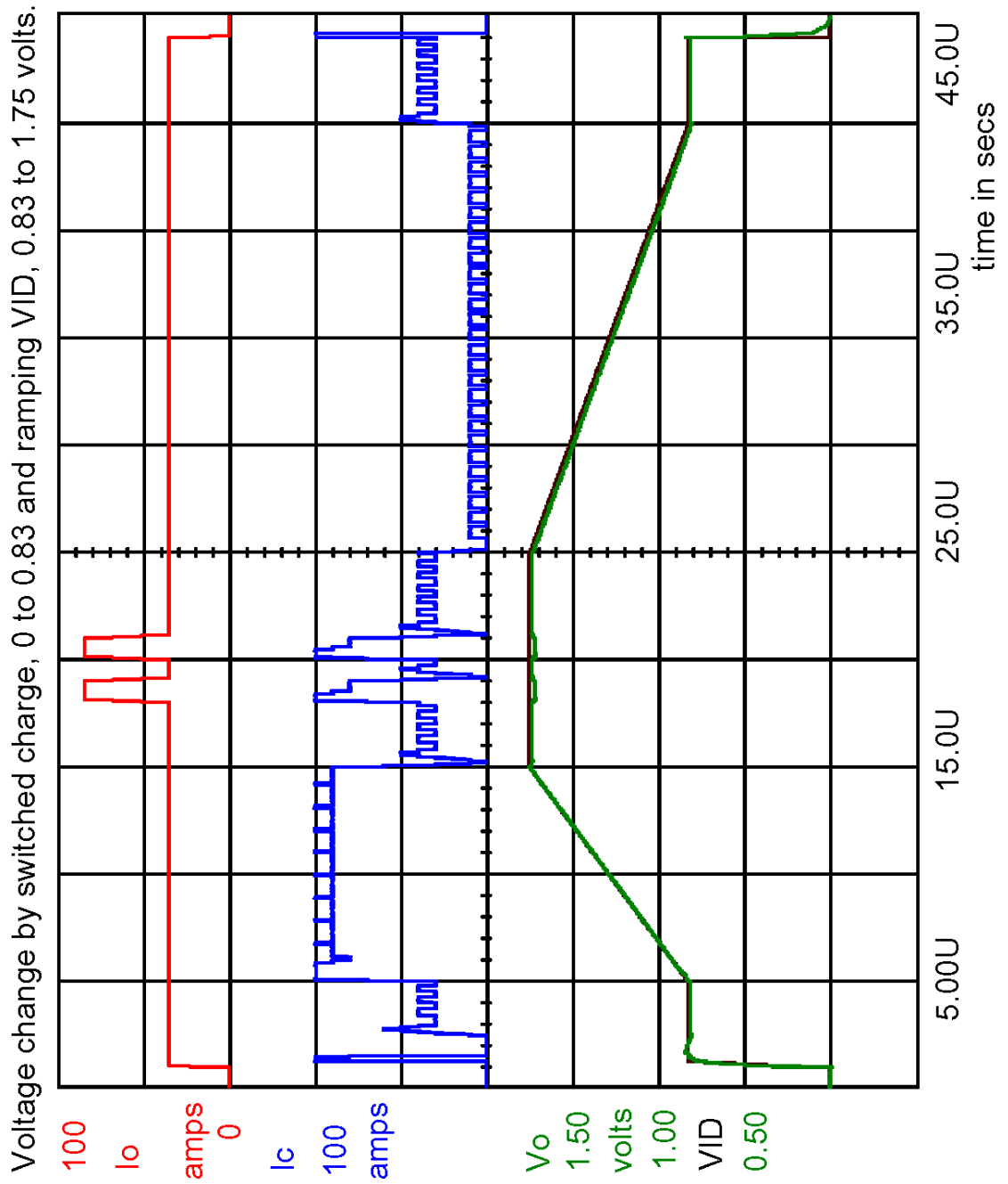
One application for a switched charge circuit is to ensure a rapid turn on. In the SPICE simulation following, a switched charge circuit adds sufficient charge to the output capacitors to step the output voltage from zero to the minimum VID voltage. From that point, voltage control is by VID ramping. At the end, the voltage is returned to zero. The voltage rises to the minimum VID in a few hundred nanoseconds without significant overshoot. Full load current is available immediately.

Because the switched charge controls the voltage step, the final output voltage depends upon the starting voltage. It may be well to include some protective circuits to ensure that the step does not occur if the starting voltage is too high. For design using a step from zero, a MOSFET clamp to ground during the off time suffices.

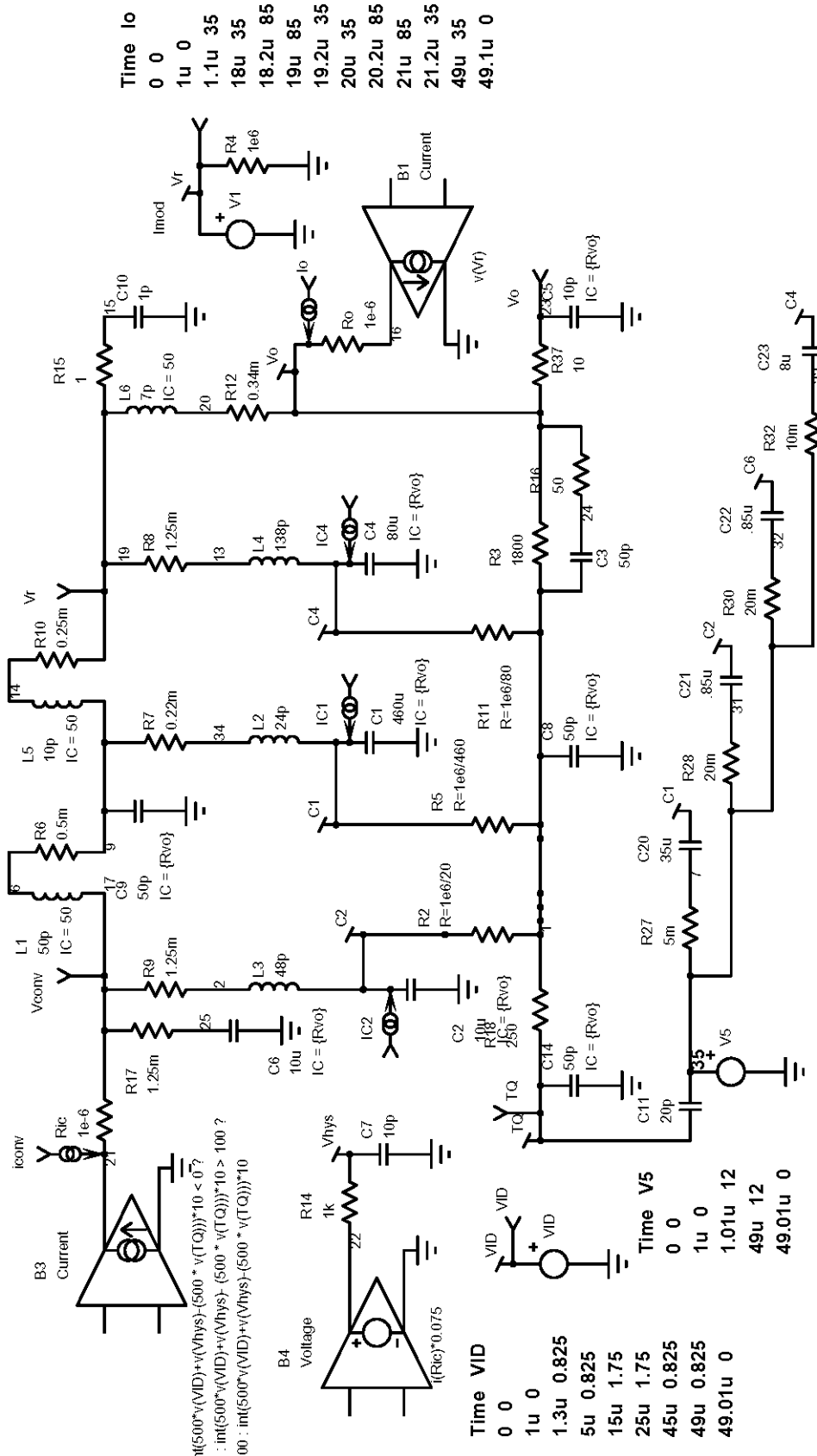
The accuracy of the voltage step requires that the capacitors have a fairly accurate relationship. The absolute accuracy is less important, but the relative accuracy determines the accuracy of the step voltage. Using the same style capacitor close together may compensate temperature effects. It may be necessary to trim the capacitors at assembly. The step voltage also depends upon the driving voltage source, so an auto-calibration is feasible, and an example is described later in this Appendix.

The SPICE schematic follows the graph. Because the switched current circuits have four capacitors separated by parasitic inductance, the totem pole driver (simulated as a controlled voltage source  $V_s$ ) drives four capacitors. It is probably sufficient to use one capacitor feeding the largest output capacitor, but the extra small capacitors are not a significant expense.





**Figure A2.3.** The output voltage is stepped from zero, then ramped by varying the VID.



Time I0  
 0 0  
 1u 0  
 1.1u 35  
 18u 35  
 18.2u 85  
 19u 85  
 19.2u 35  
 20u 35  
 20.2u 85  
 21u 85  
 21.2u 35  
 49u 35  
 49.1u 0

$\text{int}(500 \cdot v(\text{VID}) + v(\text{Vhys}) - (500 \cdot v(\text{TQ})) \cdot 10 < 0?)$   
 0 :  $\text{int}(500 \cdot v(\text{VID}) + v(\text{Vhys}) - (500 \cdot v(\text{TQ})) \cdot 10 > 100?)$   
 100 :  $\text{int}(500 \cdot v(\text{VID}) + v(\text{Vhys}) - (500 \cdot v(\text{TQ})) \cdot 10)$

Time VID  
 0 0  
 1u 0  
 1.3u 0.825  
 5u 0.825  
 15u 1.75  
 25u 1.75  
 45u 0.825  
 49u 0.825  
 49.01u 0

Time V5  
 0 0  
 1u 0  
 1.01u 12  
 49u 12  
 49.01u 0

### A2.3. Using Switched Charge for Voltage Regulator Down.

Newer processors enter a reduced voltage mode to save power. With present power supplies, this is a long and complicated process. A switched charge circuit can be used to change voltage in a discrete increment very rapidly and accurately. The switched charge circuit causes only a step in voltage; it has no ability to regulate the output voltage. Accordingly, there must be a simultaneous step change in the VID reference voltage.

The accuracy of the voltage steps is dependent upon the relative values of the capacitors. If the accuracy is uncertain, the voltage steps can be designed to be nominally somewhat low. As long as the step in the VID reference is to an accurate voltage, the output voltage will step rapidly to nearly the correct voltage, then it will ramp quickly to a very accurate final value.

Following is a SPICE simulation showing a switched current power converter having a switched charge circuit that can step the output voltage up and down about 0.4 V on command. The settling time is about 100 nsec. Three scenarios are shown, as illustrations.

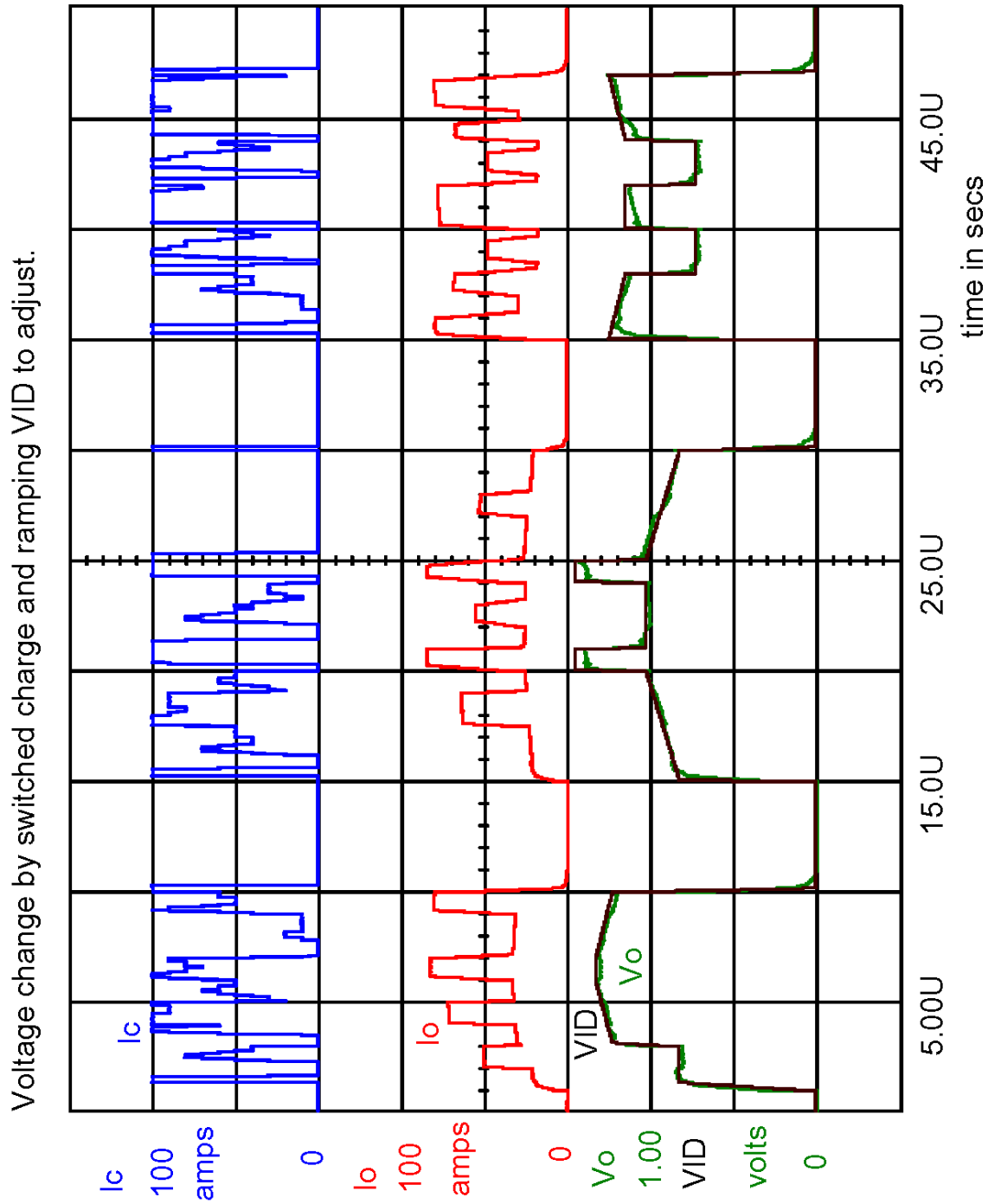
In the first, from 0 to 10  $\mu$ s, the voltage is stepped from 0 V to a minimum VID. Then it is stepped 0.4 V more, followed by a ramp up, then down. Finally, it is stepped back to 0 V. Full output current is immediately available, as can be seen in the output current trace  $I_o$ .

The next example, from 15 to 25  $\mu$ s, shows the voltage stepping from 0 V to a minimum VID, then ramping up to a working VID. When commanded, the voltage steps to a higher working VID, then back, then up again, then ramps down, then steps back to 0 V.

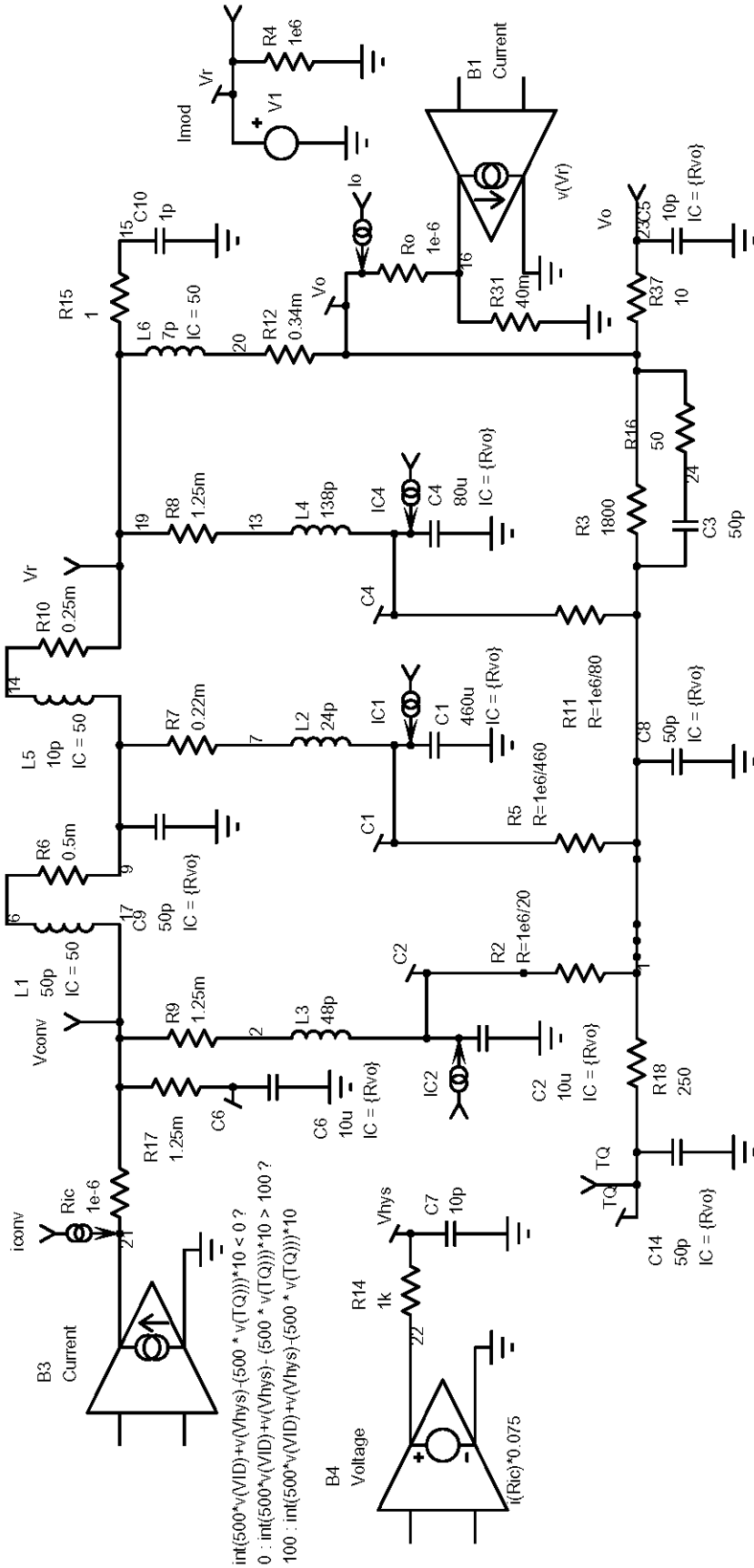
The third example shows the voltage steps commanded at the same time, so the voltage steps to the higher VID immediately. It may then ramp down somewhat, to adjust the output voltage to an optimum upper VID. From there it can step down to a lower working VID. Using both the switched charge steps and the VID ramping, any voltage within its range can be achieved.

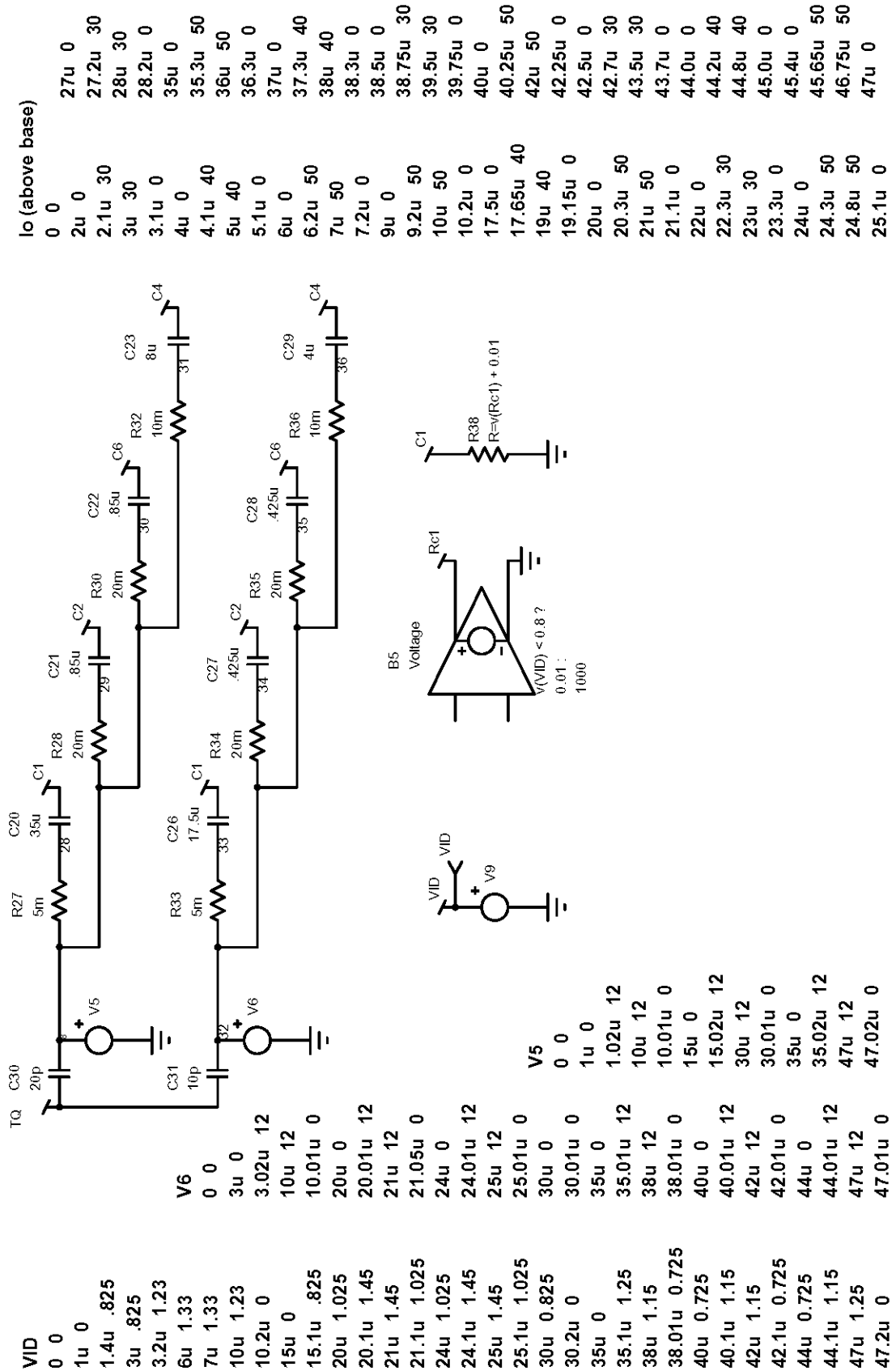
The SPICE schematic follows. Because it was getting rather busy, the schematic was divided into two pages, and the switched charge circuits are on the second page with the programmed voltage source tables. This is the SPICE model from which the graph was run. The reader is encouraged to make his own model and experiment with it.

This SPICE model includes a clamp at 0 V. Depending upon the output of the behavioral circuit B5, the resistor R38 on the second page is either 0.01  $\Omega$  or 1,000  $\Omega$ , simulating a MOSFET in its on or off state respectively. This model senses the level of the VID, but it could as well be a digital command to turn "off".



**Figure A2.5.** The output voltage is stepped using switched charge and ramped using VID.



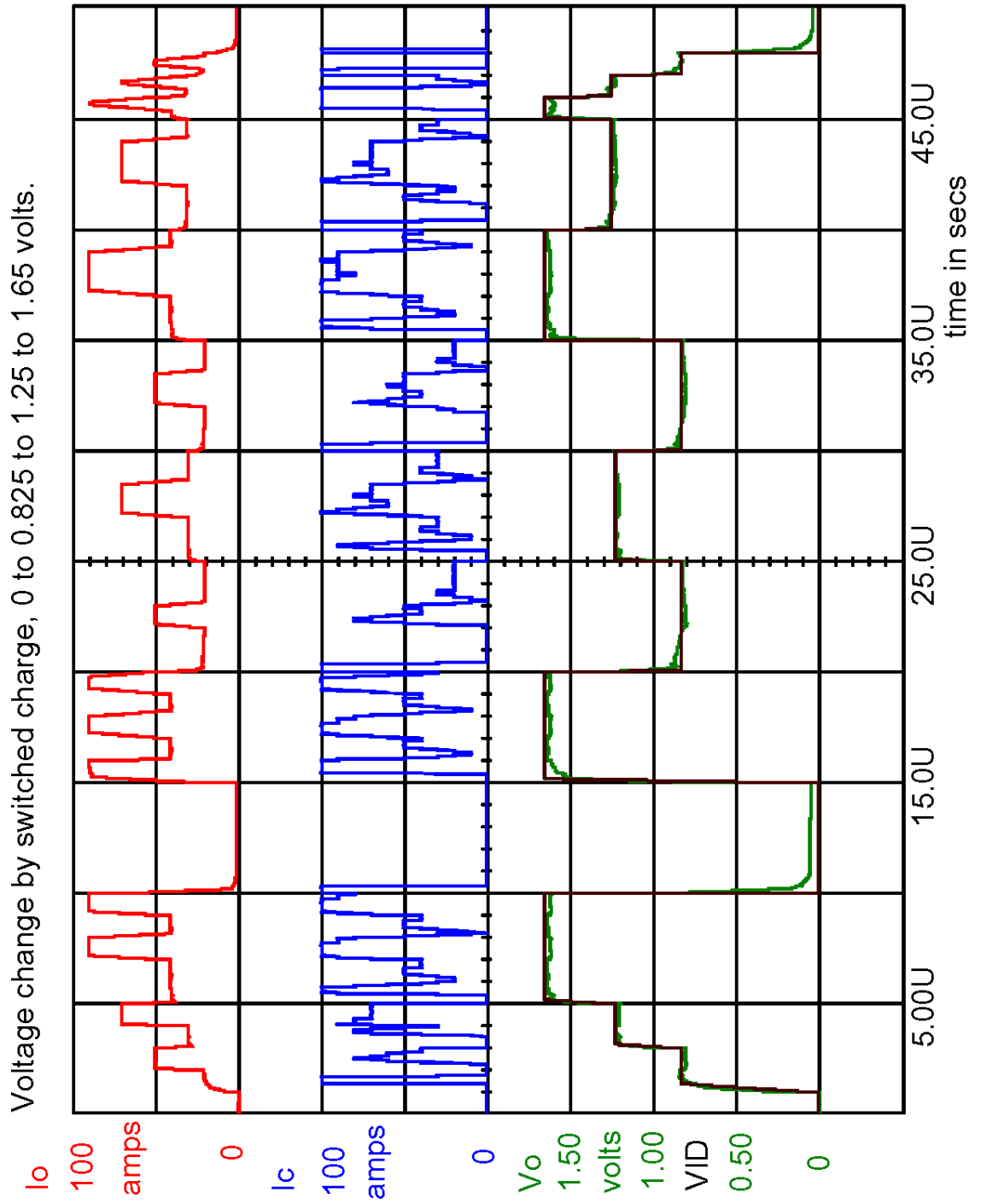


## **A2.4. Voltage Change with Multiple Switched Charge Circuits.**

For faster output voltage changes, the voltage can be changed entirely with switched charge circuits. In the example shown, the output voltage steps to a minimum VID, then there are two more increments of about 0.4 V. These can be used in any combination, superposed or sequenced, and the SPICE simulation graph following shows some representative examples. VID ramping can be used as well, but is not shown in this graph.

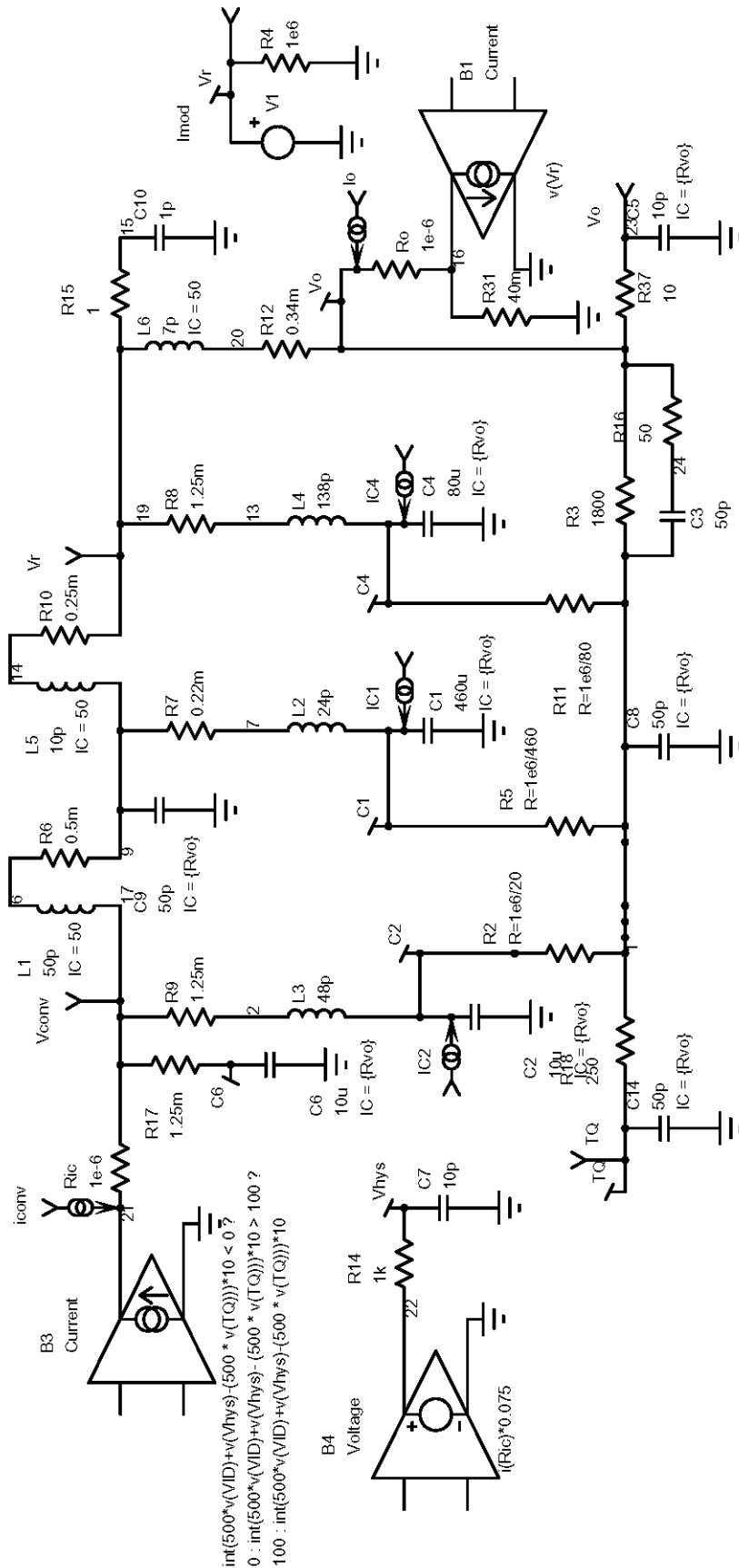
In the first scenario, from 1 to 10  $\mu$ s, the voltage steps up in three increments, in sequence, then it steps back to 0 V in one step.

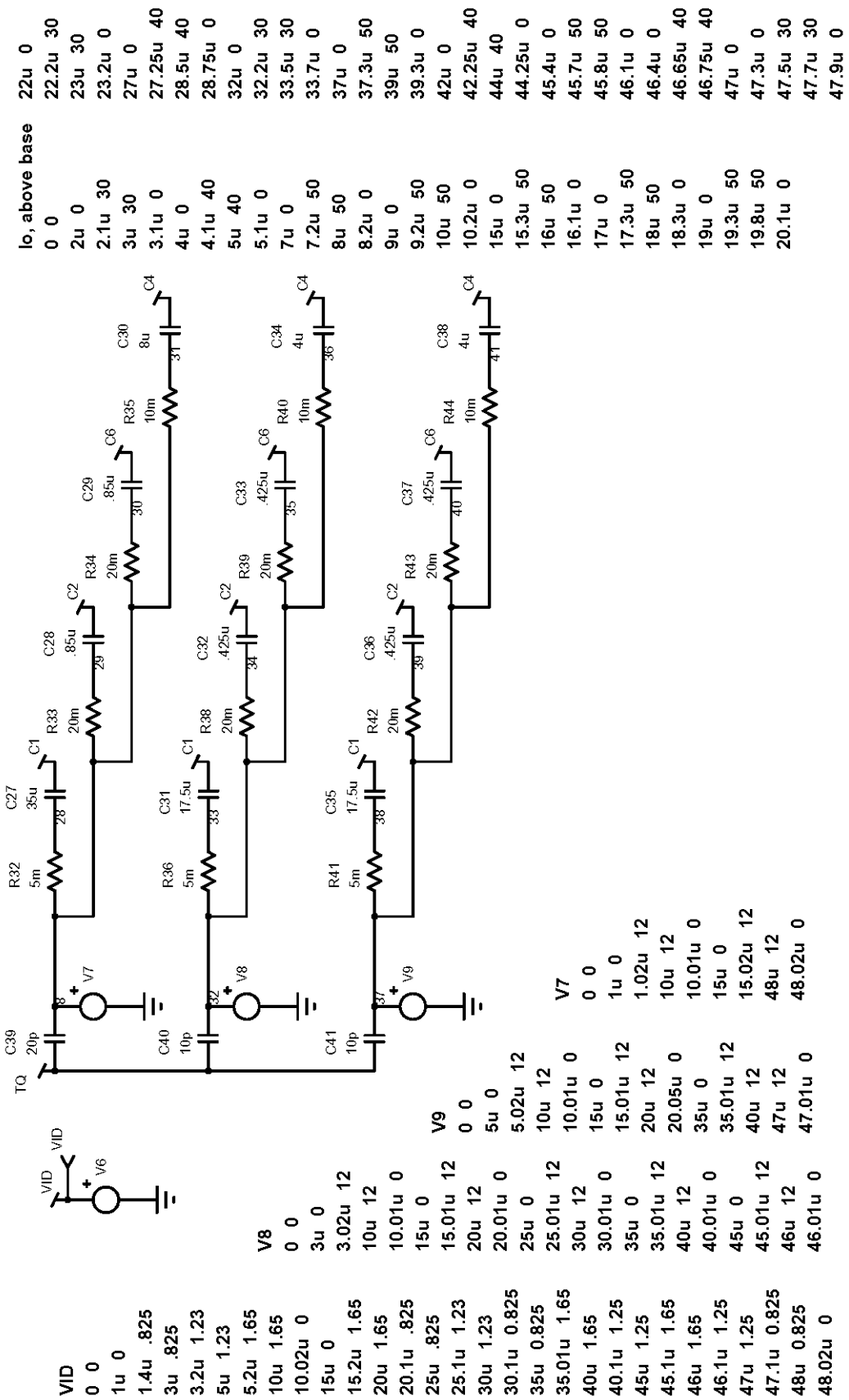
The rest of the graph shows the output voltage immediately stepping to the highest voltage, then following a number of steps as examples, finally stepping to 0 V.



**Figure A2.8.** The output voltage is stepped using stepped charge.







VID	V8	V9	Io, above base
0 0	0 0	0 0	22u 0
1u 0	3.02u 12	5u 0	22.2u 30
1.4u .825	10u 12	5.02u 12	23u 30
3u .825	10.01u 0	10u 12	23.2u 0
3.2u 1.23	15u 0	10.01u 0	27u 0
5u 1.23	15.01u 12	15u 0	27.25u 40
5.2u 1.65	20u 12	15.01u 12	28.5u 40
10u 1.65	20.01u 0	20u 12	28.75u 0
10.02u 0	25u 0	20.01u 0	32u 0
15u 0	25.01u 12	25u 0	32.2u 30
15.2u 1.65	30u 12	25.01u 12	33.5u 30
20u 1.65	30.01u 0	30u 12	33.7u 0
20.1u .825	35u 0	30.01u 0	37u 0
25u .825	35.01u 12	35u 0	37.3u 50
25.1u 1.23	40u 12	35.01u 12	39u 50
30u 1.23	40.01u 0	40u 12	39.3u 0
30.1u 0.825	45u 0	40.01u 0	42u 0
35u 0.825	45.01u 12	45u 0	42.25u 40
35.01u 1.65	46u 1.65	45.01u 12	44u 40
40u 1.65	46.1u 1.25	46u 1.65	44.25u 0
40.1u 1.25	47u 1.25	46.1u 1.25	45.4u 0
45u 1.25	47.1u 0.825	47u 1.25	45.7u 50
45.1u 1.65	48u 0.825	47.1u 0.825	45.8u 50
46u 1.65	48u 12	48u 12	46.1u 0
46.1u 1.25	46.01u 0	48.02u 0	46.4u 0
45u 0	47.01u 0		46.65u 40
47u 1.25			46.75u 40
47.1u 0.825			47u 0
48u 0.825			47.3u 0
48.02u 0			47.5u 30
			47.7u 30
			47.9u 0

## **A2.5: Binary Switched Charge SCPC.**

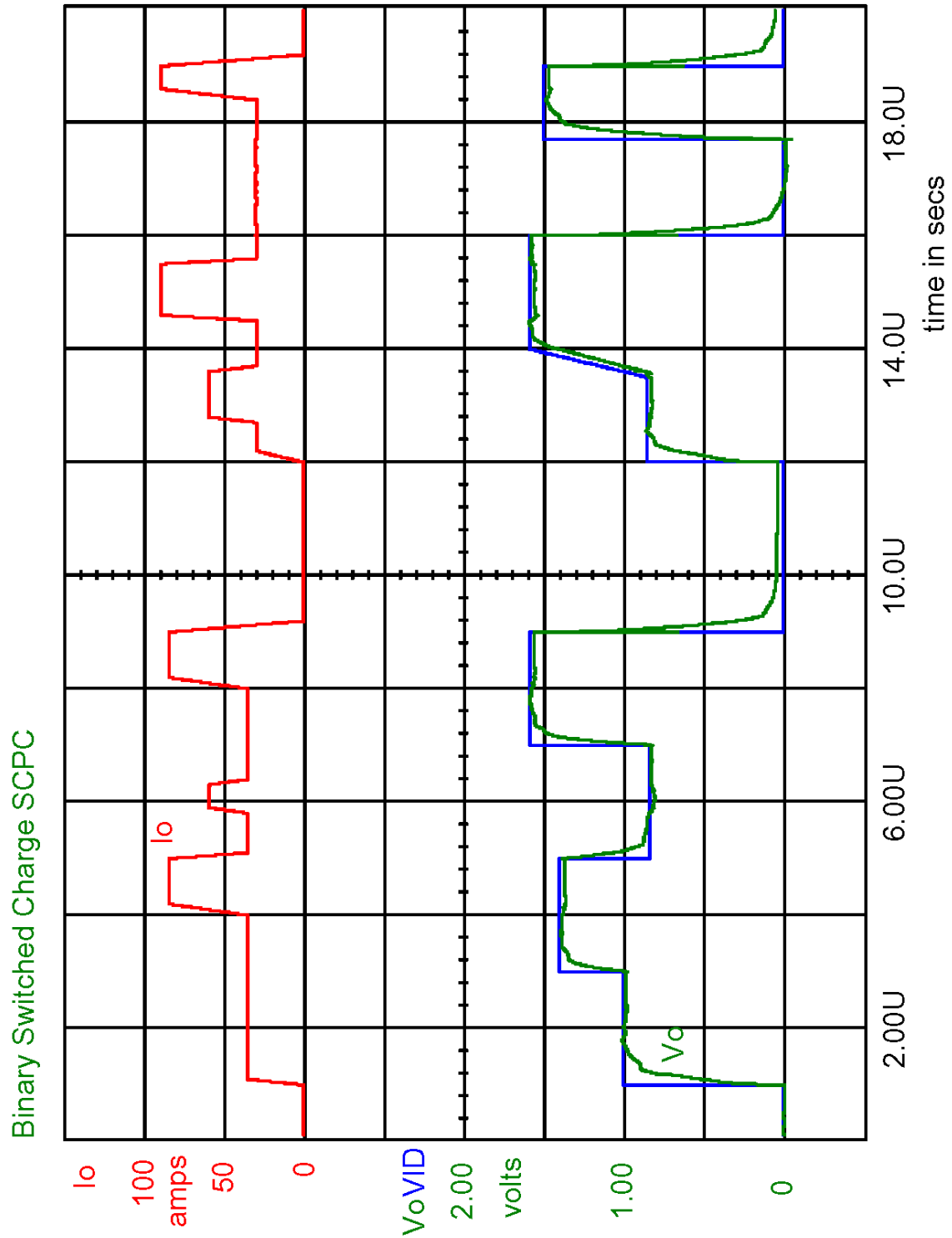
The fastest and most flexible voltage control option is the switched current power converter with a binary switched charge circuit. In the example, five switched charge circuits have a binary relationship, each subsequent switched charge circuit having half the capacitance of the previous one, so that charge is transferred to, or removed from, the output capacitor in binary increments. With five binary switched charge circuits, 32 discrete increments of voltage may be commanded, as with a VID input. In addition, a sixth switch charge circuit is used for turn on, and adds sufficient charge to the output capacitor to establish the minimum output voltage, if used alone.

Because any combination of the switches can be turned on, the output voltage can rise to any increment within its operational range upon turn on or at any time thereafter. By changing the VID binary command as a step, the voltage will step to any voltage increment within its operational range or it may be stepped to zero.

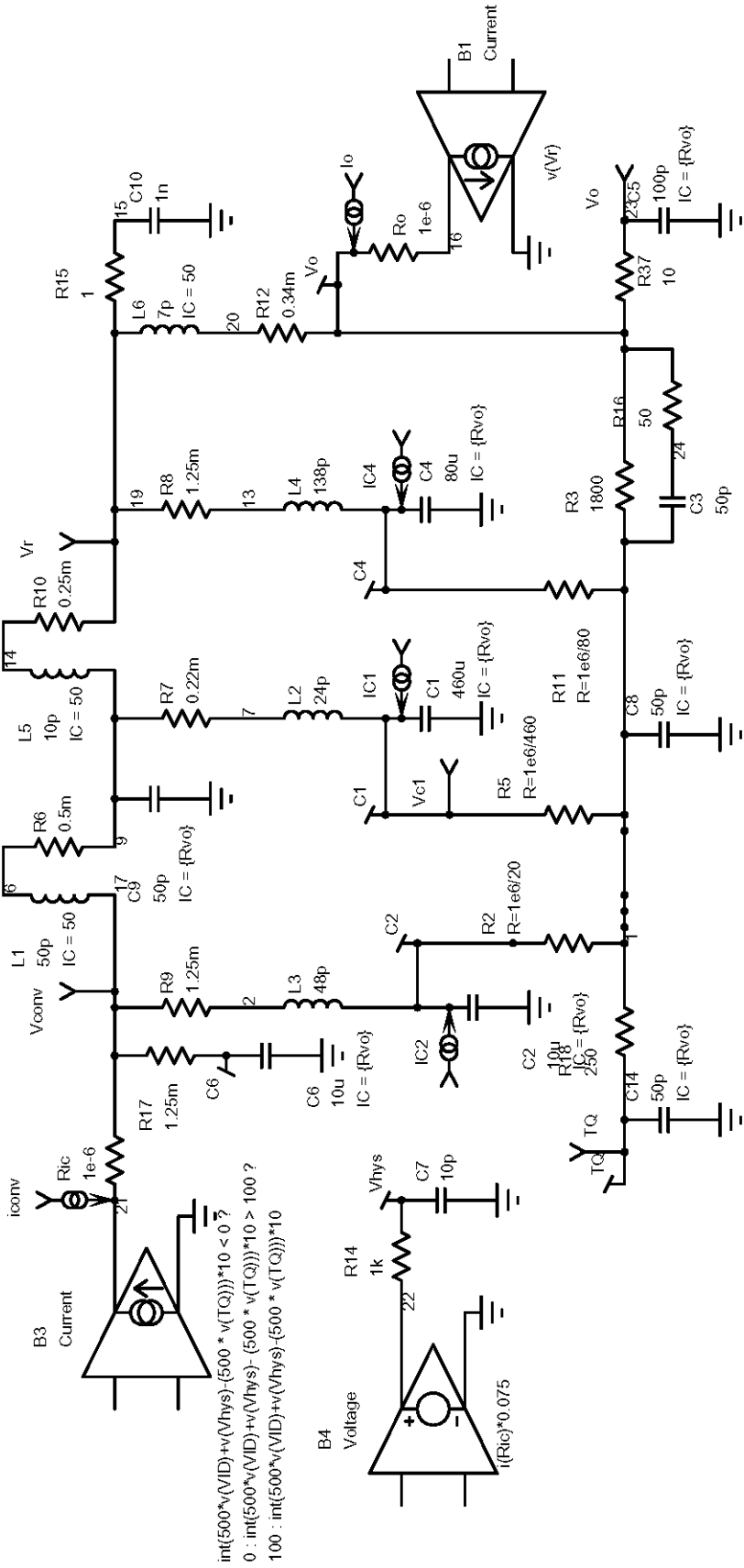
The VID binary steps may also be commanded very rapidly in binary sequence, to achieve a very fast and accurate voltage slew between the first and final binary values. This could be used to provide an appropriate output voltage for the clock rate if future processor clocks are designed to slew their frequency, with very fast changes. In the graph following, a number of scenarios are played out. Between 1 and 5  $\mu\text{s}$ , the output voltage steps, following the VID, as the load is pulsed. At 9  $\mu\text{s}$ , the voltage goes to zero simultaneously with the load going to zero. Between 13 and 14  $\mu\text{s}$ , the voltage slews very rapidly (1,600 mV/  $\mu\text{s}$ ) from the minimum to the maximum of its operational voltage range. Again at 15  $\mu\text{s}$ , it turns off.

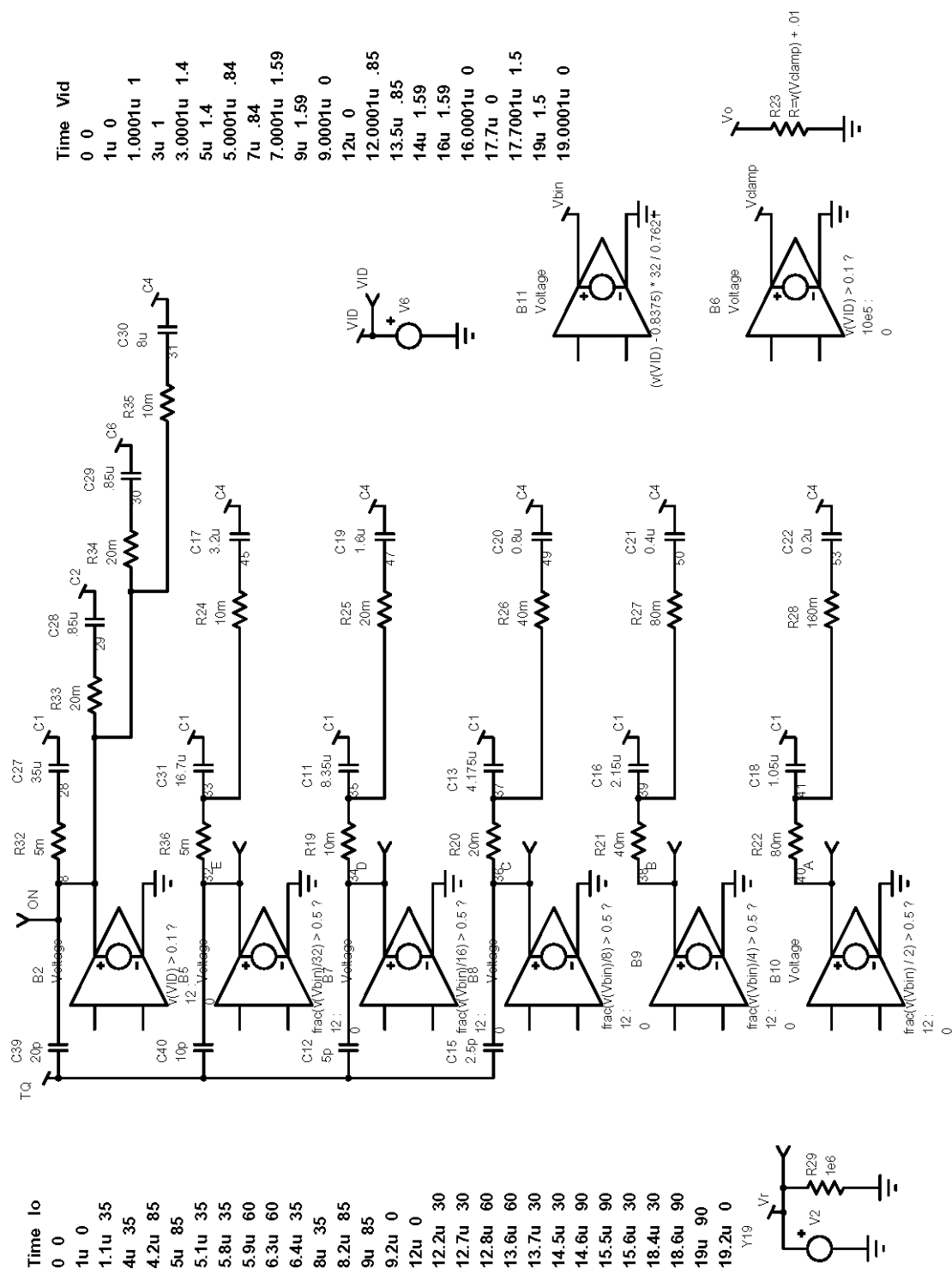
Between 17 and 19  $\mu\text{s}$ , the circuit turns on, a pulse of maximum current is applied and removed, then it turns off, all within about 1  $\frac{1}{2}$   $\mu\text{s}$ . This last scenario may be important for power reduction for a processor that has to respond rapidly and intensively when an interrupt occurs but is idle most of the time. Its net power consumption is very low, for cool operation or long battery life.

The six switched charge circuits can be seen on the second page of the SPICE model, following the graph. Note the binary sequence of the capacitor values and the series resistance of the five binary stepped charge outputs. The resistance varies so that the r-c time constants are matched.



**Figure A2.11.** The output is stepped to any VID value using binary switched charge circuits.





## **A2.6. Switch Charge Calibration:**

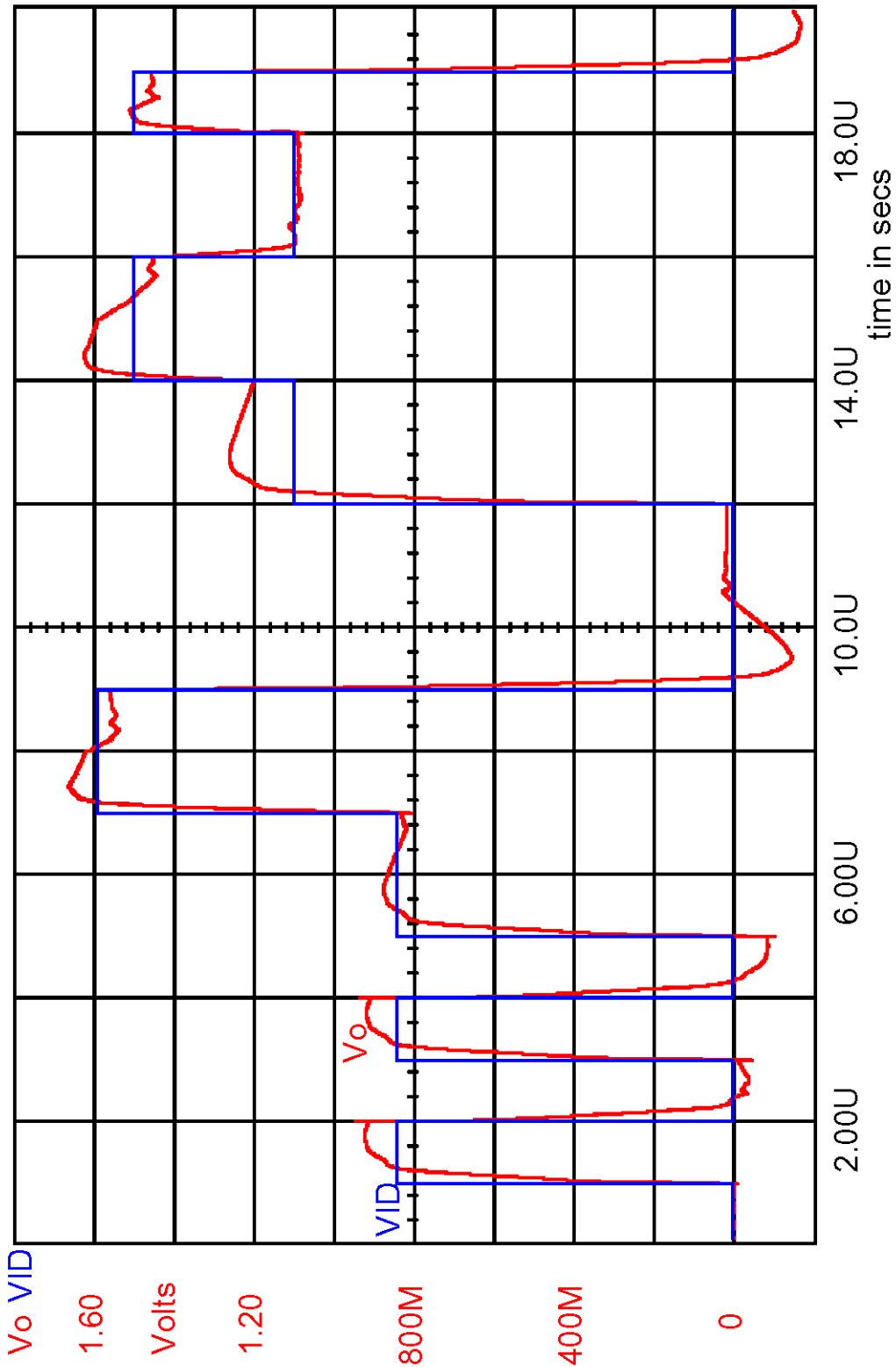
The switched charge voltage steps are only as accurate as the relative values of the capacitors if the driving voltage is fixed. Following is a graph showing the consequence of a 20 percent decrease in the size of the output capacitors. The voltage over-shoots badly, and it takes quite a while for the SCPC control to bring the output voltage back to its limit if the load current is light.

Interestingly, when an oversized capacitor was simulated, the results were much less dramatic. The voltage rose rapidly to less than its target, as expected, but then the SCPC current control was able to ramp it up quite rapidly. This suggests that the switched charge circuits should be designed nominally undersized.

For applications where it is important to have fast and accurate step voltages, the switched charge circuits may be calibrated by varying the driving voltage  $V_q$  for the switched capacitors. The graph following simulates a calibration sequence in which two test pulses are generated with the driving voltage  $V_q$  is intentionally set low. The resulting output voltage step is too low, as expected, but the level provides a calibration and the correct value can be found in just a couple of steps. The third pulse is right on.

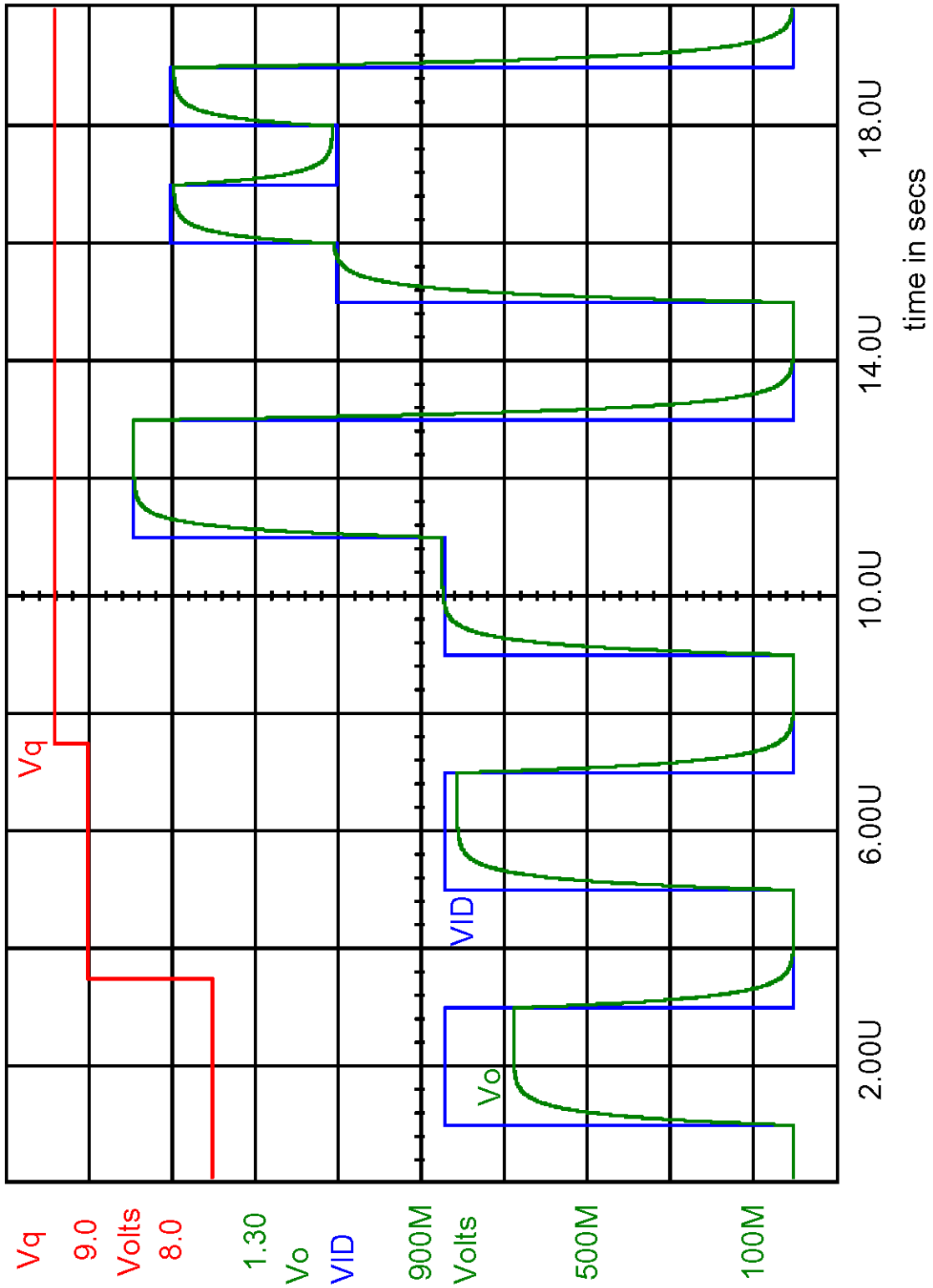
This SPICE model did not include the SCPC circuits. For one, they obscured the results, as the regulator is so fast that it alters the voltage during the time period of interest. In a practical calibration routine, the regulator could be disabled. The switched charge circuits in the SPICE model drive only the output capacitor, nothing else, up and down. The binary switching arrangement was used, and steps are shown to various levels and to zero.

A real calibration sequence could not be achieved as fast as in the SPICE model, not because of any limitation of the switched charge circuits, but because the power supply for the driving voltage will take much longer to change voltage and settle than the ideal SPICE voltage sources. However, the target  $V_q$  could be stored and used for subsequent use, perhaps recalibrating only on cold start or when an error trend is detected.

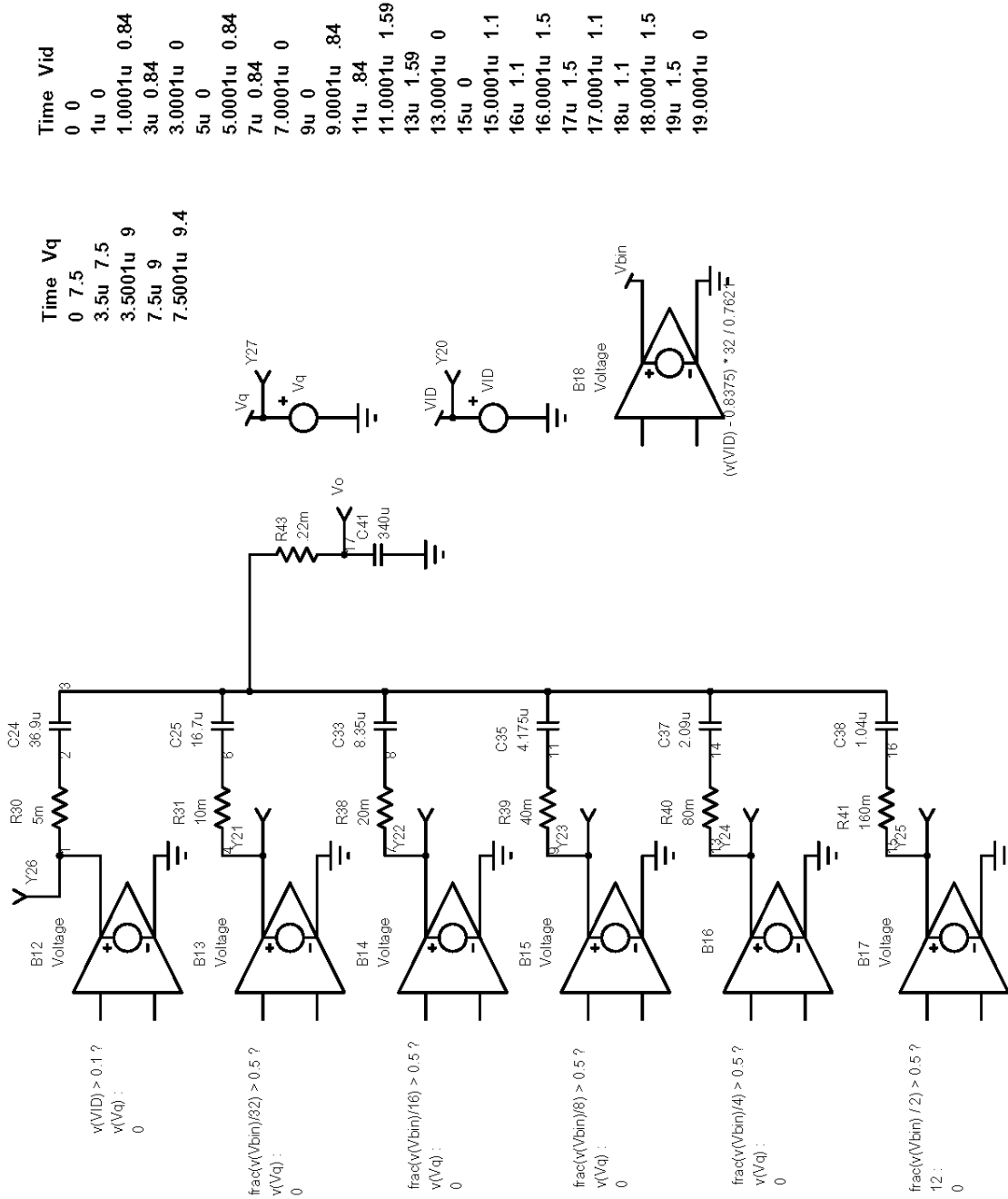


**Figure A2.14.** A condition in which the output capacitors are 20 percent undervalue is simulated. The voltage steps overshoot badly and recover slowly. Note particularly the negative voltage upon turn-off. The stepped charge circuits should be designed undersized intentionally or an auto-calibration sequence should be used to prevent this condition from occurring.





**A2.15.** A three step auto-calibration sequence successively raises test values of Vq (the driving voltage) until an accurate step is achieved, as in the third and subsequent steps.



Time	Vid
0	0
1u	0
1.0001u	0.84
3u	0.84
3.0001u	0
5u	0
5.0001u	0.84
7u	0.84
7.0001u	0
9u	0
9.0001u	.84
11u	.84
11.0001u	1.59
13u	1.59
13.0001u	0
15u	0
15.0001u	1.1
16u	1.1
16.0001u	1.5
17u	1.5
17.0001u	1.1
18u	1.1
18.0001u	1.5
19u	1.5
19.0001u	0

Time	Vq
0	7.5
3.5u	7.5
3.5001u	9
7.5u	9
7.5001u	9.4